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DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

THESIS REPORT ENTITLED

MITIGATION OF HARMONICS IN POWER DISTRIBUTION SYSTEMS USING DISTRIBUTION STATIC COMPENSATOR

BY
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DECLARATION

I declare that this thesis is my own work. It is being submitted for the degree of Master of Philosophy in Electrical and Electronic Engineering in the University of Mines and Technology (UMaT), Tarkwa. It has not been submitted for any degree or examination in any other University.

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(Signature of Candidate)

……. day of June, 2019

ABSTRACT

The quality of electric power is of major concern for both electric utilities and the end users of electric power in the wake of widespread use of nonlinear loads. Nonlinear loads normally draw non-sinusoidal (also called harmonics) currents and voltages at the point of connection with the utility grid and distribute them throughout the system causing protective relays and switchgear malfunctions, communication interference, incorrect meter readings, overheating of conductors, insulation degradation, and power transformer failures. In this research, focus was given to the harmonics generated by nonlinear loads using synchronous reference frame theory-based distribution static compensator. A distribution system having a stiff power source, linear and nonlinear loads, has been modelled in MATLAB/Simulink version 2017a software environment. For the control system design, proportional integral controllers were used for both voltage and current controls. Voltage source inverter with sinusoidal pulse width modulation was also employed for generating the alternating current. The investigation of harmonics by way of simulations, was carried out using the fast fourier transform from the MATLAB software to evaluate the total harmonic distortion generated by the nonlinear load with and without DSTATCOM connected. The simulation results indicated that at steady state voltage values of V_{dc} of 489 V, 555 V and 575 V, the current THD stood at 5.71%, 6.89% and 6.26%, respectively after mitigation giving a minimum of 55.8% reduction of harmonics in the source current. The distribution static compensator stands to be recommended for current harmonics mitigation in low voltage distribution systems.

DEDICATION

To God Be the Glory

This thesis report is dedicated to the following:

My son

Ethan Senam Dzah

My wife

Doris Mawufemor Adukpoh – Dzah

My parents

Mr Fritz K. Dzah and Mrs Sesime Kumah Dzah

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This thesis work has been completed not by my strength but through the grace of God, for He has been my support and protector throughout the programme.

At this point of my career, I know I am indebted to many individuals for their support, encouragement and guidance. I would therefore like to express my heartfelt gratitude to my gallant supervisors Dr Francis B. Effah and Mr Erwin Normanyo. Their guidance, technical discussions and constant encouragements accompanied with patience have actually helped me in the completion of this work. It is true that, their immense experience and understanding of the topic helped me in tackling some of the difficult challenges encountered in doing this research work. I thank them for all that they have done for me. I would like to acknowledge Dr Solomon Nunoo who is also the Head of Department, Electrical and Electronic Engineering, for his effort and countless enlightening conversations which led to the achievement of this goal. To all lecturers in the Electrical and Electronic Engineering Department, I say, thank you for the knowledge impacted in me.

Nothing in life is possible without the love and support from one's family. I would therefore like to express my sincere gratitude to my lovely wife Doris Mawufemor Adukpoh for her sacrifices, patience, support and unconditional love. I would like to express my undying love and gratitude to my mother Sesime Kumah Dzah (Mrs) and father Fritz K. Dzah for their lifetime support, encouragement and education. Their love and blessings made everything I have accomplished possible. I would also like to thank all my siblings for their prayers, constant support in diverse ways and encouragement. Last but not the least, I would like to express my gratitude to all my course mates for their support. May the almighty God continue to guard and guide each and every one of us for a better future.

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LIST OF ABBREVIATIONS

Abbreviation	Meaning
AC	Alternating Current
BFOA	Bacteria Foraging Optimisation Algorithm
CCM	Current Control Mode
CPD	Custom Power Device
CSI	Current Source Inverter
DC	Direct Current
DCLV	DC Link Voltage
DSTATCOM	Distribution Static Compensator
DVR	Dynamic Voltage Restorer
ECG	Electricity Company of Ghana
FACTS	Flexible Alternating Current Transmission Systems
FFT	Fast Fourier Transform
GSA	Gravitational Search Algorithm
HAPF	Hybrid Active Power Filter
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated Gate Bipolar Transistor
IRP	Instantaneous Reactive Power
LCL	Inductor Capacitor Inductor
LPF	Low Pass Filter
LSPWM	Level Shifted Pulse Width Modulation
MCPWM	Multi-Carrier Pulse Width Modulation
MLI	Multilevel Inverter
NPC	Neutral Point Clamped
PCC	Point of Common Coupling
PI	Proportional Integral
PID	Proportional Integral Derivative
PLL	Phase Locked Loop
PQ	Power Quality
PR	Proportional Resonance

PSO	Particle Swarm Optimisation
PSPWM	Phase Shifted Pulse Width Modulation
PWM	Pulse Width Modulation
SAPF	Shunt Active Power Filter
SCR	Silicon Control Rectifier
SPWM	Sinusoidal Pulse with Modulation
SRF	Synchronous Reference Frame
SVC	Static Var Compensator
TDD	Total Demand Distortion
THC	Total Harmonic Current
THD	Total Harmonic Distortion
THD_I	Total Harmonic Current Distortion
THD_V	Total Harmonic Voltage Distortion
UPQC	Unified Power Quality Compensator
VSC	Voltage Source Converter
VSI	Voltage Source Inverter

LIST OF SYMBOLS

Amplitude of the current harmonic	I_n
Amplitude of the fundamental current	I_1
Actual output signal	Y(s)
Angular frequency of the waveform	ω
Cycle that start working the controller	n
Current drawn by the rectifier	I_r
Current ripple factor	I_{crp}
Controller output signal	U(s)
Desired input signal	R(s)
DC voltage	V_{dc}
Derivative gain	K_d
DC current	I_{dc}
DC link charging current	i_{dc}
DC capacitor	C_{dc}
Damping coefficient	ξ
Error	e
Equalizing resistance	R_E
Fundamental frequency	f_o
Full Load fundamental current	I_L
Filter current	I_F
Harmonic frequency	f_h
Harmonic component in the load current of the d – axis	I_{dh}
Instantaneous current supply	i_S
Instantaneous load current	i_L
Instantaneous converter current	i_C
Integral gain	K_i
Integral gain of voltage	K_{iv}

Instantaneous direct current	i_d
Instantaneous quadrature current	i_q
Injected current	I_{inj}
Integer number	h
Interface inductor	L_f
Interface resistor	R_f
Line – to – line grid voltage	V_{LL}
Load current in the α - axis	$I_{L\alpha}$
Load current in the β - axis	$I_{L\beta}$
Load current in the d – axis	I_{Ld}
Load current in the q – axis	I_{Lq}
Modulation index	m
Number of output voltage levels	N_L
Number of switches	N_S
Number of voltage sources	S
Natural frequency	ω_n
Overloading factor	a
Phase difference	ϕ
Proportional gain	K_p
Proportional gain of voltage	K_{pv}
Power rating of the system	S_n
Peak value of the grid phase voltage	V_m
Quadrature load current	I_{Lq}
Quadrature reference current	I_{q_ref}
Quadrature voltage	V_q
Reference dc current	I_{dc_ref}
Reference dc voltage	V_{dc_ref}

Reference current	I_{ref}
rms AC voltage	V_{ar} (rms)
Source current	I_S
Source voltage	V_S
Source impedance	Z_S
Source resistance	R_S
Source reactance	X_S
Source inductance	L_S
Switching frequency	f_s
Total AC current drawn by rectifier and R–L load	I_t
Transformation angle	θ
Time period of the system	T
Voltage drop	V_{dp}
Voltage available to the load	V_o
Voltage at the PCC	V_{tpcc}
Voltage in the d – axis	V_d
Voltage in the q – axis	V_q

INTERNATIONAL SYSTEM OF UNITS (SI UNITS)

Quantity	Unit	Symbol
Time	seconds	s
Frequency	hertz	Hz
Electric current	ampere	A
Electric potential	volt	V
Electric resistance	ohm	Ω
Electric capacitance	farad	F
Inductance	henry	H

CHAPTER 1

GENERAL INTRODUCTION

1.1 Background to the Research

A pure sinusoidal waveform with zero harmonic distortion is said to be a hypothetical quantity and not practical. The reason being that, even the voltage waveform at the point of generation, contains small amounts of distortion due to non-uniformity in the excitation magnetic field and discrete spatial distribution of coils around the generator stator slots. The distortion at the point of generation is usually very low, typically less than 1.0% (Basim, 2017). The generated voltage is transmitted many hundreds of kilometers, transformed to several levels, and finally distributed to the power consumer. The main objective of the electric utility is to deliver sinusoidal voltage at fairly constant magnitude throughout their system (Jaisiva *et al*., 2016). The user equipment generates currents that are rich in harmonic frequency components, especially in large commercial or industrial installations. As harmonic currents travel to the power source, the current distortion results into additional voltage distortion due to impedance voltages associated with the various power distribution equipment, such as distribution lines, transformers, cables, and buses. The harmonic distortion is the major source of sine waveform distortion (Priya *et al*., 2016).

Harmonics are the major source of sinusoidal waveform distortion. Harmonics have become more common in power systems now. Harmonic distortion is caused by nonlinear loads in power systems (Ali *et al*., 2016). Nonlinear loads are referred to as loads in which the current is not proportional to the applied voltage (Jaisiva *et al*., 2016). In short, harmonics are integral multiples of the fundamental frequency of the sinusoidal wave that is, harmonics are multiples of the 50 Hz or 60 Hz fundamental voltage and current.

According to Fourier theory, a periodic waveform can be expressed as a sum of pure sine waves of different amplitudes where the frequency of each sinusoid is an integer multiple of the fundamental frequency of the periodic waveform (Jaisiva *et al*., 2016). A frequency that is an integer multiple of the fundamental frequency is called harmonic frequency, i.e. $f_h = hf_o$ where f_o and h are the fundamental frequency and an integer number, respectively.

Harmonics in power systems can lead to system failure if not mitigated. The following are some of the ways by which harmonics may affect the power distribution system (Eyad, 2016):

i. Overheating of conductors;
ii. Failure of capacitor due to heat rise;
iii. False operations and tripping of fuses and circuit breakers;
iv. Excessive overheating in the transformer;
v. Interference and operation instability of generators;
vi. Utility meters may record measurements incorrectly, resulting in higher billings to consumers;
vii. Harmonics can cause failure of the commutation circuits, found in DC drives and AC drives with Silicon Controlled Rectifiers (SCRs); and
viii. Computers/telephones may experience interference or failures.

Distribution Static Compensator (DSTATCOM) is the most effective device that can be used in mitigating harmonics in distribution systems (Priya *et al*., 2016). The primary function of the DSTATCOM is to control the reactive power and also to regulate voltage. It was found that voltage fluctuations were reduced from 2.5% to 0.2% by the use of DSTATCOM (Rani and Jyothi, 2011). This reduces voltage flicker substantially (Bhim *et al*., 2015; Padiyar, 2007). Therefore, in this research, DSTATCOM will be used as a device for mitigating harmonics in order to unravel the effect of harmonics in power distribution systems. In Ghana, the frequency of power generated is 50 Hz therefore this frequency will be considered in this thesis report.

1.2 Problem Definition

In reality, the supplied voltage to customers' equipment and the resulting load currents are supposed to be perfect sine waves. But in practice, however, since conditions sometimes are never ideal, these waveforms are often in one way or the other distorted. This deviation from the perfect sinusoidal waveform is usually expressed in terms of harmonic distortion of the voltage and current waveforms. Harmonic distortion in power systems has become a major concern due to the fact that some devices or equipment used by consumers generate currents that are rich in harmonic frequency components such as harmonic current, in large

commercial or industrial installations. The effects of harmonics are classified into four main categories such as (Snehal and Dnyaneshwar, 2016):

i. Power system itself;
ii. Consumer load;
iii. Communication circuits; and
iv. Revenue billing.

In power systems, harmonic currents are the main cause of equipment overheating. The impact is worse when network resonances amplify harmonic currents. Harmonics may also interfere with relaying and metering to some degree. Harmonics can lead to thyristor firing errors in converters and Static Var Compensator (SVC) installations, metering inaccuracies, and false tripping of protective devices. The performance of consumer equipment, such as motor drives and computer power supplies, can be adversely affected by harmonics. In addition, harmonic currents flowing in power lines can induce noise on nearby communication lines.

Harmonic voltage distortion may cause equipment insulation stress, particularly in capacitors. When harmonics cause the voltage impressed on the capacitor bank to be distorted, the peak voltage may be high enough to cause a partial discharge, or corona, within the capacitor dielectric. This may eventually result in a short circuit at the edges of the foil and failure of the capacitor bank. Figure 1.1 (Anon., 2014) illustrates harmonic waveforms superimposed on the fundamental frequency signal. Also, Figure 1.2 (Anon., 2014) illustrates distorted wave composed by the superposition of a 50 Hz fundamental and 3^{rd} and 5^{th} harmonics.

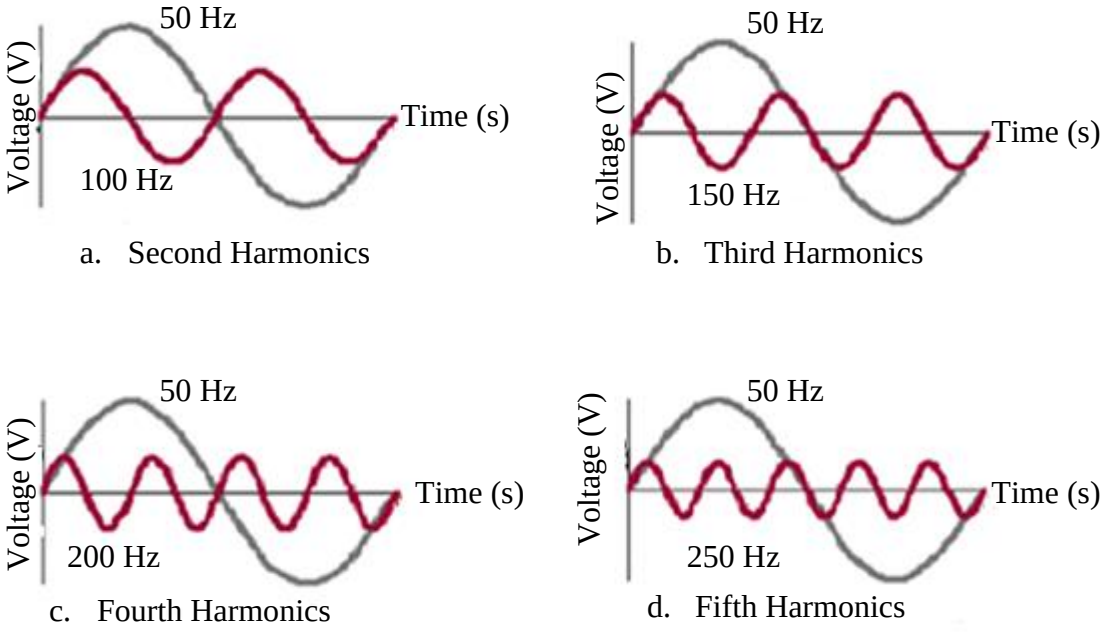

Figure 1.1 Harmonic Waveforms Superimposed on the Fundamental Frequency Signal

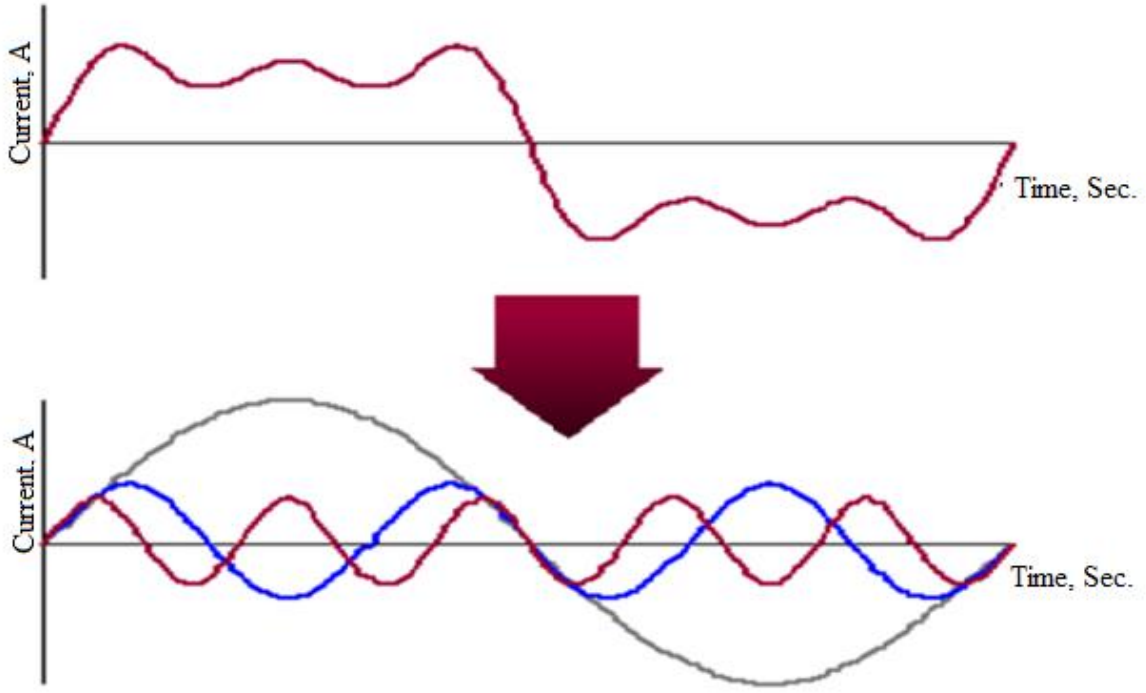

Figure 1.2 Distorted Wave Composed by the Superposition of a 50 Hz Fundamental and 3rd and 5th Harmonics

1.3 Purpose of the Research

The purpose of this research is to utilise a Custom Power Device (CPD) in solving a current-based power quality problem in electric power distribution system.

1.4 Objectives of the Research

The main objective of this research is to mitigate harmonics in power distribution systems using DSTATCOM. This can be achieved through the following specific objectives:

i. To develop control algorithm for the DSTATCOM implementation; and
ii. To validate the use of DSTATCOM in mitigating the inherent high harmonic content in power distribution system through modelling and computer simulations using MATLAB/Simulink power system environment.

1.5 Expected Outcomes

At the end of this research, the expectations are that:

i. There will be a DSTATCOM-based device which when connected to the distribution system will reduce the harmonic content;
ii. The effect of harmonic distortion in distribution systems can be reduced; and
iii. The problem of power quality which is due to harmonics can be reduced.

1.6 Research Questions and Hypothesis

This research is being guided by the following questions:

i. What are harmonics distortion in electric power distribution systems?
ii. Can high harmonic content in power distribution systems be reduced using DSTATCOM?

The research hypothesis is stated as follows: The inherent high harmonic content in electric power distribution systems can be mitigated to acceptable levels using DSTATCOM.

1.7 Scope of the Research

This research work is limited to 400 volts electric power distribution systems, which is used to send power to consumer's premises. The main issue is to solve the current related power quality problem of harmonics associated with power distribution systems in Ghana. With this, the focus of this work is to mitigate current harmonics which normally return to the source of supply before resulting into voltage harmonics.

1.8 Research Methods Used

The research methods employed include the following:

i. Review of related literature that are in the domain of the research topic from books, journals and other recognized publications;
ii. Modelling of the power and control circuits of the DSTATCOM; and
iii. Computer simulations using MATLAB/Simulink power system environment.

1.9 Facilities Used for the Research

Facilities used for this research work include:

i. Internet, Library, Laboratory and Computer Facilities at UMaT and Ho Technical University; and
ii. Laptop Computer with MATLAB/Simulink Software.

1.10 Significance of the Research

Harmonic distortion is still the most significant power quality problem in power systems. High harmonic content in power systems can cause damage to transformers, cables, capacitor banks, failure of protective devices and can interfere with the energy meters leading to high bills to customers. Therefore, this research will help find solutions to various effects associated with harmonic distortion. More also, it will serve utility companies such as Power Distribution Services (PDS) Ghana, from spending more money on damaged equipment due to harmonics and also the consumers' from receiving high electricity bills.

1.11 Limitations of the Research

The limitation of this research is that, the conclusions drawn from this research are only based on the simulation results, without practical implementation of the system.

1.12 Definition of Terms and Key Concepts

Harmonic component: It is the component of order greater than one of the Fourier series of a periodic quantity.

Harmonic content: It is the quantity obtained by subtracting the fundamental component from an alternating quantity.

Harmonic distortion: It is the periodic distortion of the sine wave.

Harmonic filter: It is a device for filtering one or more harmonics from the power system. Active and passive filters are the most commonly used harmonic filters.

Harmonic number: It is the integral number given by the ratio of the frequency of a harmonic to the fundamental frequency.

Harmonic resonance: It is the condition in which the power system is resonating near one of the major harmonics being produced by nonlinear elements in the system, thus exacerbating the harmonic distortion.

Impulsive transient: It is a sudden, non-power frequency change in the steady-state condition of voltage or current that is unidirectional in polarity (primarily either positive or negative).

Instantaneous: It is used to quantify the duration of a short-duration variation as a modifier. This term refers to a time range from one-half cycle to 30 cycles of the power frequency.

Interharmonic component: It is a frequency component of a periodic quantity that is not an integer multiple of the frequency at which the supply system is designed to operate (e.g., 50 or 60 Hz).

Inverter: It is a power electronic device that converts direct current to alternating current of either power frequency or a frequency required by an industrial process.

Linear load: It is an electrical load device that, in steady-state operation, presents essentially constant load impedance to the power source throughout the cycle of applied voltage.

Nonlinear load: It is an electrical load that draws current discontinuously or presents impedance that varies throughout the cycle of the input ac voltage waveform.

Notch: It is a switching (or other) disturbance of the normal power voltage waveform, lasting less than a half-cycle, which is initially of opposite polarity than the waveform and is thus subtracted from the normal waveform in terms of the peak value of the disturbance voltage.

Total demand distortion: It is the ratio of the root mean square of the harmonic current to the rms value of the rated or maximum demand fundamental current, expressed as a percentage.

Total harmonic distortion: It is the ratio of the root mean square of the harmonic content to the rms value of the fundamental quantity, expressed as a percentage of the fundamental.

Pulse-width modulation: It is a common technique used in inverters to create an ac waveform by controlling the electronic switch to produce varying width pulses.

Overvoltage: It is used to describe a specific type of long-duration variation, and refers to a voltage having a value of at least 10 percent above the nominal voltage for a period of time greater than one minute.

Passive filter: It is the combination of inductors, capacitors, and/or resistors designed to eliminate one or more harmonics. The most common variety is simply an inductor in series with a shunt capacitor, which short-circuits the major distorting harmonic component from the system.

Active filter: This type of filter uses power electronic switching to generate harmonic current that cancel the harmonic current from a nonlinear load.

Hybrid filter: It is based on the combination of active and passive filters. Such a combination with the passive filter makes it possible to significantly reduce the rating of the active filter.

Phase shift: It is the displacement in time of one voltage waveform relative to other voltage waveform(s).

Point of common coupling: Point on a public power supply system, electrically nearest to a particular load, at which other loads are, or could be, connected. It is a point located upstream of the considered installation.

1.13 Organisation of the Thesis

This thesis work consists of five chapters arranged as follows:

Chapter 1 covers background to the research, problem definition, purpose of the research, objectives of the research, expected outcomes, research questions and hypothesis, scope of the research, research methods used, facilities used for the research, significance of the research, limitations of the research, definition of terms and key concepts.

Chapter 2 reviews the literature on harmonic mitigation methods for power distribution systems. It also discusses the use of Custom Power Devices (CPD) with the control algorithms and filters.

Chapter 3 covers the research methodology and focuses on general description of the system, power distribution system, DSTATCOM for harmonic mitigation, design of the control system and computer simulations.

Chapter 4 gives the results, discussions and the summary of findings.

Chapter 5 covers the conclusions, recommendations, research contributions and future research directions.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter of the thesis actually discusses and reviews contributions of other researchers in the domain of the research topic. This is done in order to acquire more knowledge about the research topic chosen, the concepts involved and any other related information in order to improve upon the already existing works. The review is centered on harmonics in power distribution systems; harmonic mitigation techniques; power electronic converters for harmonics mitigation; custom power devices and control system for the mitigation of harmonics.

2.2 Harmonics in Power Distribution Systems

Generally, power distribution systems in Ghana are designed to operate at a fundamental frequency of 50 Hz. However, there are certain types of loads that produce currents and voltages with frequencies that are integer multiples of the 50 Hz. These higher frequencies are a form of electrical pollution known as power system harmonics. Harmonics are generated by any load, which draws current not proportional to the voltage applied. Most loads are to some extent nonlinear, but some generate more and higher level of harmonics than others.

A “linear” load connected to an electric power system is defined as a load which draws current from the supply which is proportional to the applied voltage. A load is considered to be “nonlinear” if its impedance changes with the applied voltage. Due to the change in impedance, the current drawn by the nonlinear load is also nonlinear i.e. non-sinusoidal in nature, even when it is connected to a sinusoidal voltage source.

The main difference between linear and nonlinear loads is that, linear loads absorb electrical power linearly hence, their current waveforms remain sinusoidal in nature whereas non-linear loads absorb electrical power in a nonlinear manner hence the current drawn by them becomes non-sinusoidal in nature and therefore, distorted (Contractor *et al*., 2015).

2.2.1 Definition of Harmonics

Harmonic component in a power distribution system can be defined as the sinusoidal component of a periodic waveform that has a frequency equal to an integer multiple of the fundamental frequency of the system f_h = h × fundamental frequency, where h is the integer to be multiplied. Periodic waveforms occurring at frequencies of 2f, 4f, 6f, 8f etc. are called even harmonics; whiles those with frequencies of 3f, 5f, 7f, 9f etc. are called odd harmonics. Although, harmonics are classified as even and odd harmonics, even harmonics get cancelled due to their symmetrical nature whiles odd harmonics remain in the system and need to be eliminated by the method of filtering or compensation techniques. Figure 2.1 (Ramon, 2015) illustrates typical voltage harmonic waveforms due to nonlinear loads.

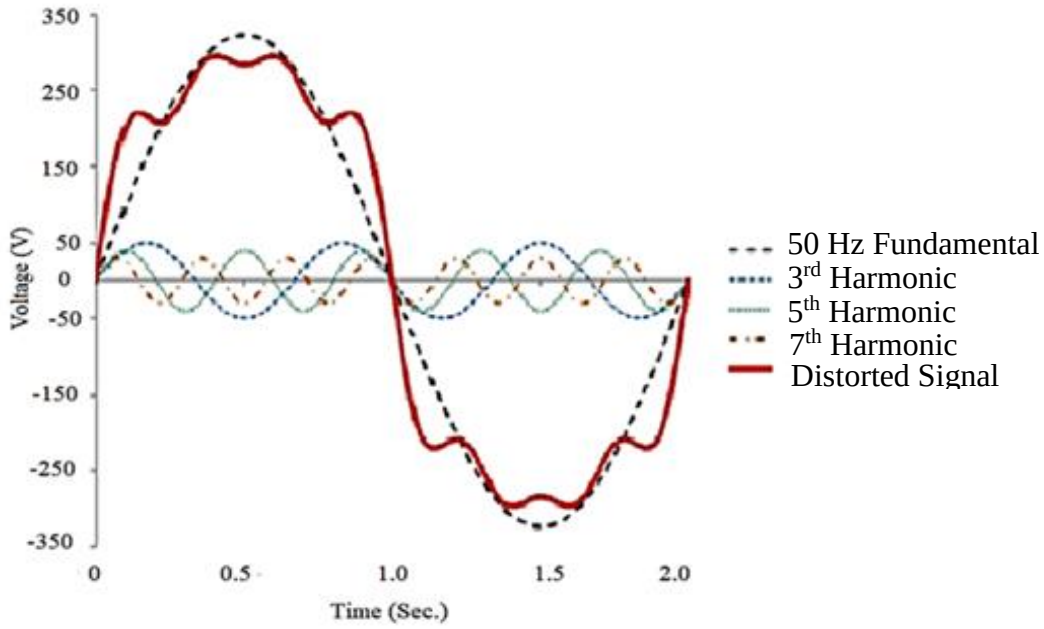

Figure 2.1 Voltage Harmonic Waveforms as a Result of Nonlinear Loads

2.2.2 Harmonic Current

A load is considered nonlinear if the current drawn by the load will not be sinusoidal even when it is connected to a sinusoidal voltage. In this case such nonlinear current contains frequency components that are multiples of the power system frequency (Kamenka, 2014). Harmonics current are therefore caused by these nonlinear loads which lead to the disruption of the desired linear system. Figure 2.2 (Snehal and Dnyaneshwar, 2016) illustrates a typical non-sinusoidal nature of current waveform caused by nonlinear load.

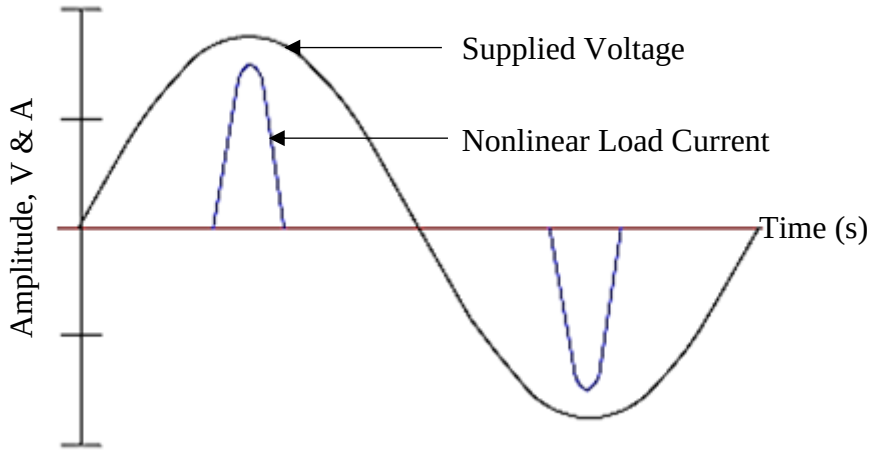

Figure 2.2 Typical Current Waveform due to Nonlinear Load

2.2.3 Harmonic Voltage

Voltage harmonics are caused by the current harmonics which distort the voltage waveform (Snehal and Dnyaneshwar, 2016). These harmonic currents interact with the impedance of the electrical power network to create voltage distortion that can affect the power network itself and the loads connected to it (Anon., 2014a). These voltage harmonics affect the entire system not just the loads which are causing them. The impact of voltage harmonics depends on the distance of the load causing the harmonics from the power source.

2.2.4 Harmonic Distortion

In this modern world with changing technology, a few number of industries use rectifiers or converters, power supplies and other electronic devices to improve upon the quality of their products. These electronic devices introduce the distortion of the smooth sinusoidal wave of the supply current. This will actually make the flow of current not to be directly proportional to the supply voltage. These loads are often referred to as nonlinear loads. The non-linear loads usually lead to waveforms that are multiples of the fundamental frequency sine wave to be superimposed on the base (design) waveform. Hence, the frequency of the second harmonic is two times the fundamental and that of the third harmonics is three times the fundamental. Therefore, the combination of the sine wave with all the harmonics creates a new non–sinusoidal wave of entirely different shape, referred to as harmonic distortion.

2.2.5 Harmonic Phase Sequences

Harmonics of different orders are said to have different phase sequences. In general terms, a phase sequence is the order of rotation of phase vectors relative to each other. Positive sequence harmonics have the same phase rotation as the fundamental component (i.e. 4^{th}, 7^{th}, 10^{th}, ...). These harmonics circulate between the phases. Negative sequence harmonics have the opposite phase rotation with respect to the fundamental component (i.e. 2^{nd}, 5^{th}, 8^{th}). These harmonics also circulate between the phases. Zero sequence harmonics do not produce a rotating field. These harmonics circulate between the phase and neutral or ground (i.e. 3^{rd}, 6^{th}, 9^{th},) unlike positive and negative sequence harmonics.

2.2.6 Triplen Harmonics

Triplen harmonics are the odd integer multiples of the third harmonic waveform. Triplen harmonics are of particular concern because they are zero sequence harmonics. Electronic equipment generates more than one harmonic frequency. Some of these electronic equipment generate harmonics such as 3^{rd}, 9^{th}, 15^{th} and 21^{st} etc. Such harmonics are referred to as triplen harmonics. Triplen harmonics can do more harm than distortion of voltage waveforms; hence it has been recognised as a major concern to both engineers and building designers. This is because triplen harmonics can lead to overheating of wiring in buildings, nuisance tripping, overheating of transformer units, and random end-user equipment failure.

2.2.7 Harmonic Indices

Harmonic indices are the index values developed for assessing the quality of current and voltage waveforms due to the presence of harmonics. The two most commonly used indices for measuring the harmonic content of a waveform are the total harmonic distortion and total demand distortion. Harmonic component in power systems can be calculated for, by considering it as a percentage of the fundamental or a percentage of the root mean square (rms) value of the total current as shown in Equation (2.1) (Kamenka, 2014).

$$I_h = \frac{I_n}{I_1} \times 100\ \% \qquad (2.1)$$

where, I_n = amplitude of the current harmonic in amperes

I_1 = amplitude of the fundamental current (or rms value of the total current) in amperes

Equation (2.1) can be applied to harmonic voltage as well.

Total harmonic distortion

Total Harmonic Distortion (THD) is the term used to describe the level of harmonic content in the power distribution system. It is therefore defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. The THD value is normally used for low, medium, and high voltage systems.

Total harmonic current

Total Harmonic Current **(**THC**)** is the accumulated currents of the orders 2 to 40 that contribute to the distortion of the current waveform. This value is particularly useful in determining the required characteristics for installation of modern active harmonic filters (Kamenka, 2014). The expression for THC is given in Equation (2.2) (Kamenka, 2014).

$$THC = \sqrt{\sum_{n=2}^{n=40} I_h^2} \qquad (2.2)$$

Total harmonic distortion of current

Total Harmonic Distortion of current (THD_I) usually specifies the total harmonic current distortion of the waveform. This value is defined as the percentage ratio of the harmonic current to the fundamental (non-harmonic) current measured at a load point at the particular moment when the measurement is taken. For example, the sum of all the current harmonics being calculated in relation to the fundamental frequency current up to the 40^{th} harmonic order can be calculated as shown in Equation (2.3) (Kamenka, 2014).

$$THD_I = \frac{\sqrt{\sum_{n=2}^{n=40} I_h^2}}{I_1} \times 100\% = \frac{\sqrt{I_{h2}^2 + I_{h3}^2 + ...+ I_{hn}^2}}{I_{h1}} \times 100\% = \frac{THC}{I_1} \qquad (2.3)$$

Total harmonic distortion of voltage

The Total Harmonic Distortion of voltage (THD_V) also specifies the total magnitude of the voltage distortion. This value is also defined as the percentage ratio of the harmonic voltage to the fundamental (non-harmonic) voltage. Equation (2.4) (Kamenka, 2014) expresses the sum of all the voltage harmonics being calculated in relation to the fundamental frequency voltage up to the 40^{th} harmonic order.

$$THD_V = \frac{\sqrt{\sum_{n=2}^{n=40} V_h^2}}{V_1} \times 100\% = \frac{\sqrt{V_{h2}^2 + V_{h3}^2 + ... + V_{hn}^2}}{V_{h1}} \times 100\ \% \qquad (2.4)$$

Total demand distortion

Total Demand Distortion (TDD) is the ratio of the measured harmonic current to the full load fundamental current. The full load fundamental current is the total amount of non-harmonic current consumed by all the loads on the system when the system is at peak demand. So the TDD is the THD of current being normalised to the maximum demand load current. TDD is equal to THDi only if the system is at full load condition. The expression of the TDD is as presented in Equation (2.5) (Kamenka, 2014).

$$TDD = \frac{\sqrt{\sum_{n=2}^{n=40} I_h^2}}{I_L} \times 100\% = \frac{\sqrt{I_{h2}^2 + I_{h3}^2 + ... + I_{hn}^2}}{I_L} \times 100\% \qquad (2.5)$$

2.3 Harmonics Filtering Techniques

Filters are mainly employed in power systems in order to reduce excessive harmonics in the system. The major technique of employing harmonic filters is to utilise power electronic switches to produce equal and opposite current signals that eliminate the harmonic currents from the nonlinear loads (Ekhlas *et al.*, 2015). The resulting effect of harmonics being injected into the power system due to the rapid increase in consumers' nonlinear load calls for a greater concern. The technique is to install filters that can suppress or interact with the power system harmonic (Mikkili and Panda, 2016). In general, harmonic filters can be classified as passive or active filters. Passive filtering technique is most commonly used in industries because it provides a low impedance path to harmonic currents over a certain

frequency bandwidth and also cheaper in cost. The more sophisticated active filtering concepts operate in a wider frequency range (De La Rosa, 2015). Active filters are designed to inject harmonic currents to counterbalance existing harmonic components as they show up in the distribution system. Active filters comprise of DC, AC, series, and parallel configurations. Hybrid filters are a combination of passive and active filtering schemes. The harmonic components in the system usually are of a very large magnitude of current. Compensation of harmonics can therefore be achieved by the use of filters (Contractor *et al.*, 2015).

2.3.1 Passive Filtering of Harmonics

Passive filters are filter circuits that are tuned to a specific frequency, which means that this filter circuit offers a high impedance path to the fundamental frequency and a low impedance path to ground for the higher specific frequencies (Sahana, 2015). Passive filters cannot be used in power systems where the harmonic component keeps changing or varies randomly (Mikkili and Panda, 2016). Passive filters are generally classified into three main categories as passive series, passive shunt and passive hybrid filters. The choice of any of these configurations depends on the level of harmonic content in the system and most importantly, the advantages of each of them. The use of passive filters has the advantage of reducing undesirable harmonics in the system and also provide reactive power compensation in order to improve the system performance. The disadvantage of using these filters is that, it allows the occurrence of resonance with line impedance. Also, it requires a lot of calculations since tuning frequency is less accurate and also, they are heavy and bulky. Figure 2.3 (Sahana, 2015) shows a schematic diagram of the connection of passive filters.

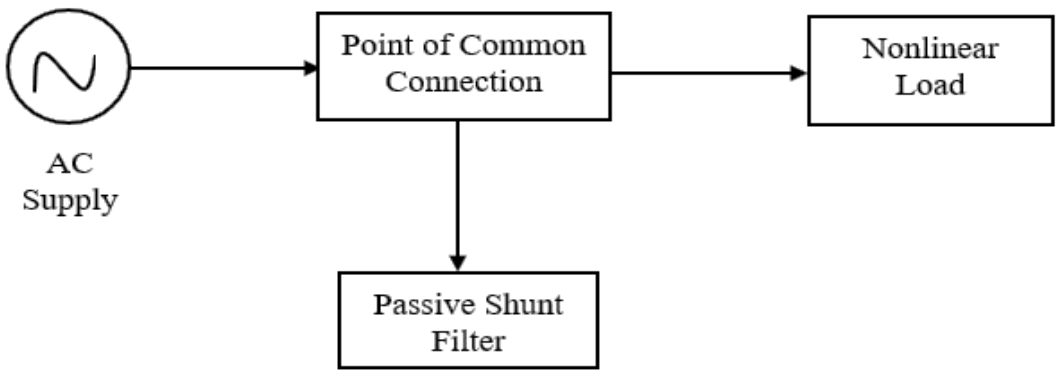

Figure 2.3 Schematic Diagram of the Connection of Passive Filter

2.3.2 Active Filtering of Harmonics

Active filters are filter circuits which in their operation monitor continuously the harmonic current being generated by the nonlinear loads and hence generate exactly the same waveform corresponding to the load. In short, active filters inject equal and opposite harmonics into the power system to cancel those generated by the nonlinear loads (De La Rosa, 2015; Mikkili and Panda, 2016). The basic principle of active filters is based on the utilisation of power electronic technologies for generating the required harmonic level which can cancel that produced by the nonlinear load. The merits of active filters are as follows: Ability to cancel out harmonics, block resonance, management of reactive power, accurate and easy tuning, small size and more importantly, they can be used when harmonic component keeps changing or varies randomly. Unlike passive filters, active filters are very expensive and also, there is a possibility of developing inherent harmonics due to the power electronic devices. Active filters are classified into three main categories namely; shunt active, series active and hybrid active filters. Shunt active filters can further be classified based on the type of converter, topology and the number of phases. The converter used can either be current source converter or voltage source converter (Bhim *et al*., 2015). Figure 2.4 (Sahana, 2015) shows a schematic diagram of active shunt filter with nonlinear load.

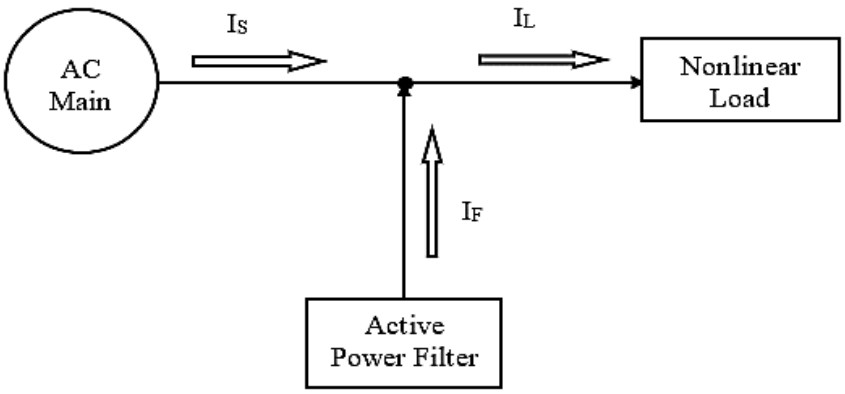

Figure 2.4 Schematic Diagram of Active Shunt Filter with Nonlinear Load

2.3.3 Hybrid Harmonic Filter

Hybrid harmonic filter is a type of filter circuit which is designed by combining both passive and active filter circuits together for filtering harmonic components in power systems. Hybrid harmonic filters are used in power systems where passive filters can be used for

constant or static loads whereby that of active filters can be used for mitigating harmonics produced by randomly changing loads. The combined circuit is generally referred to as Hybrid Active Power Filter (HAPF) (Rooh *et al*., 2015). Figure 2.5 (Bhim *et al*., 2015) shows a schematic diagram of hybrid power filter as a combination of active shunt and passive shunt filters. Hybrid power filters have a very large number of configurations each of which depends on the non-linear load present in the system. Among a lot, only four of these configurations are mostly used due to a number of benefits and also, in order to meet the requirements of various types of nonlinear loads. These four configurations are: A combination of passive series and passive shunt filters, a combination of series connected passive shunt and active shunt filters, a combination of active series and passive shunt filters and a combination of active series and active shunt filters.

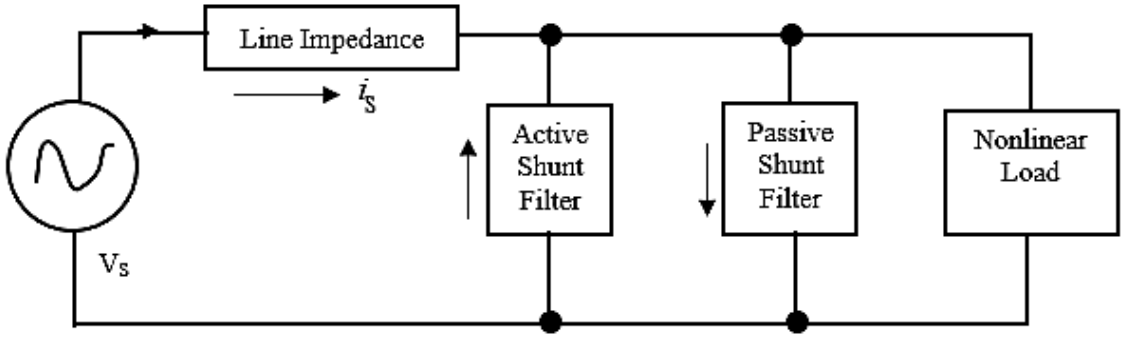

Figure 2.5 Schematic Diagram of Hybrid Power Filter as a Combination of Active Shunt and Passive Shunt Filters

2.4 Two-Level Voltage Source Converter for Harmonic Mitigation

Voltage Source Converter (VSC) is the type of circuit that permits the conversion from dc voltage source to ac voltage output and it is often referred to as inverter (Euzeli and Edison, 2015). In this circuit design, a dc capacitor is normally provided at the dc source side which stabilises the dc voltage. The 2-level converter is capable of generating two output voltage levels by switching between, $+V_{dc}$ and $-V_{dc}$ (Anaya-Lara *et al*., 2014). Even though the circuit design of the converter is simple with small sizes of dc capacitor, its basic output ac waveform contains high harmonic content and also has higher switching frequency due to the dc capacitor size which leads to higher switching losses. For medium and high-voltage applications, Pulse Width Modulation (PWM)-based two-level converters are limited due to current and voltage ratings of the switching devices (Das, 2015).

In order to overcome the effect of harmonics, multilevel converters were introduced. Multilevel converters (inverters) are capable of offering better performance than the conventional two-level converters (Andrzej, 2016). The multilevel converter has the advantages of low pulse height, reduced harmonic content and lower switching frequency with much lower switching power losses (Yuriy *et al*., 2016). The use of multilevel converter improves the quality of the ac output voltage generated. This is because with multilevel converters, the quality of the output voltage increases as the number of voltage levels increases. Figure 2.6 (Karthikeyan *et al*., 2014; Euzeli and Edison, 2015) shows the schematic diagram of a three phase two-level voltage source converter.

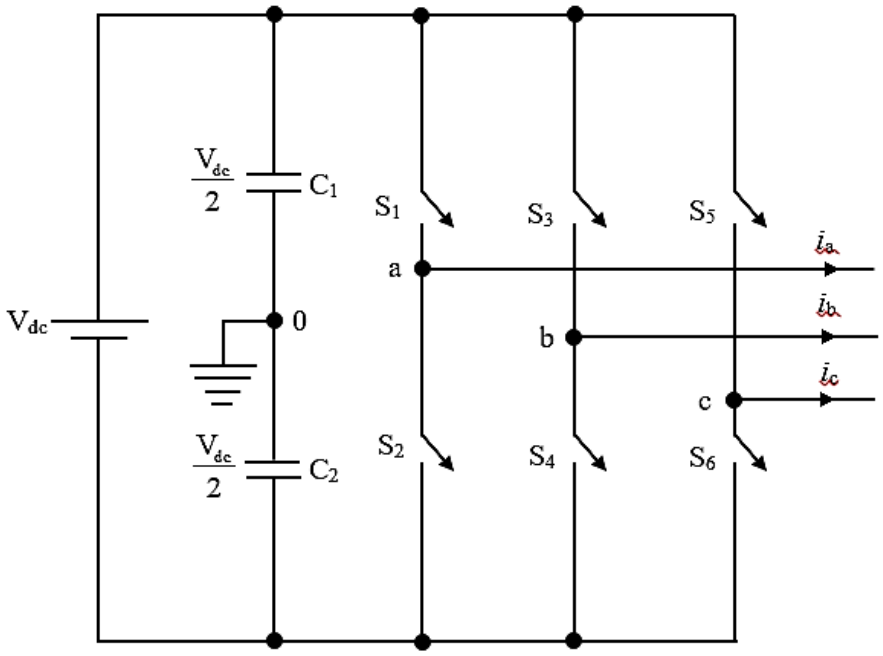

Figure 2.6 Three Phase Two-Level Voltage Source Converter

2.5 Multilevel Converter for Harmonic Mitigation

Multilevel inverter is a power electronic device which is capable of providing the desired alternating voltage level at the output where DC voltage is taken as the input. A dc to ac power conversion is performed by inverter circuits. These inverter circuits are usually supplied from a DC source whiles its output is an AC voltage which has a fundamental component with adjustable frequency and magnitude. Inverters can be classified according to the type of source and these are: Voltage Source Inverter (VSI) and Current Source Inverter (CSI). Active power filters for harmonic current mitigation in a power system

represent an example of dc-to-ac power conversion. Multilevel converters (i.e. dc to ac inverters) offer better performance than two-level inverters (Andrzej, 2016). The performance of a multilevel inverter in terms of ratings, efficiency and operation mainly depends on its topology and the type of control algorithm used in its PWM controller (Gaddafi *et al*., 2016). The most commonly used multilevel inverter topologies are: Diode clamped and flying capacitor topologies for single source multilevel inverters, and then the H-Bridge for the multi-source case. The H-bridge multilevel inverter can be cascaded, hybrid or new hybrid. The mitigation of harmonics is usually achieved through the switching design (i.e. switching angles are calculated in a special way) of the multilevel inverters when considering the various topologies. Figure 2.7 (Murugesan *et al*., 2016) shows the types of multilevel inverter topologies.

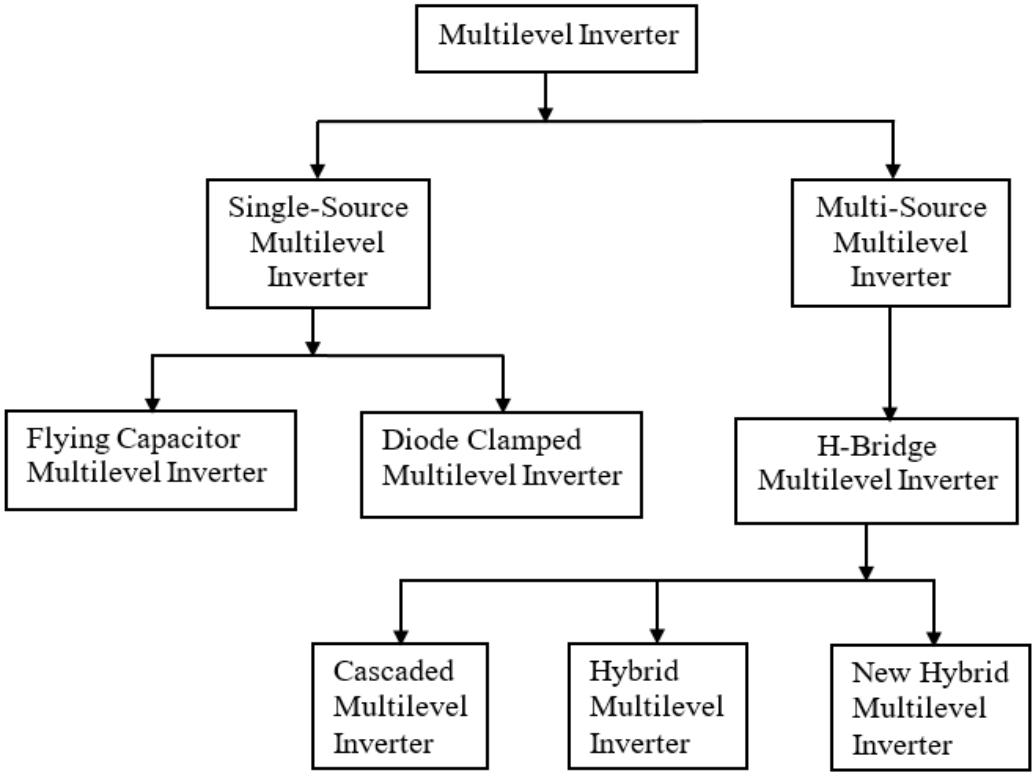

Figure 2.7 Types of Multilevel Inverter Topologies

2.5.1 Diode Clamped Multilevel Inverter

The diode clamped type of multilevel inverter uses capacitors in series to divide the DC bus voltage into a set of voltage levels. To produce n-levels of the phase voltage, an n-level diode clamped multilevel inverter needs n-1 capacitors on the DC bus. For a DC bus voltage

of V_{dc}, the voltage across each capacitor will be $V_{dc}/3$ (Gaddafi *et al*., 2016). The main advantage of this type of multilevel inverter is that in terms of three phase system, the entire phases share a common dc bus, which minimises the capacitance requirements of the converter. The main disadvantage is that real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control. The number of clamping diodes required is by calculation related to the number of levels, which can also be cumbersome for units with a higher number of levels. Figure 2.8 (Euzeli and Edison, 2015) shows the schematic diagram of three level diode (or neutral) clamped inverter with voltage source.

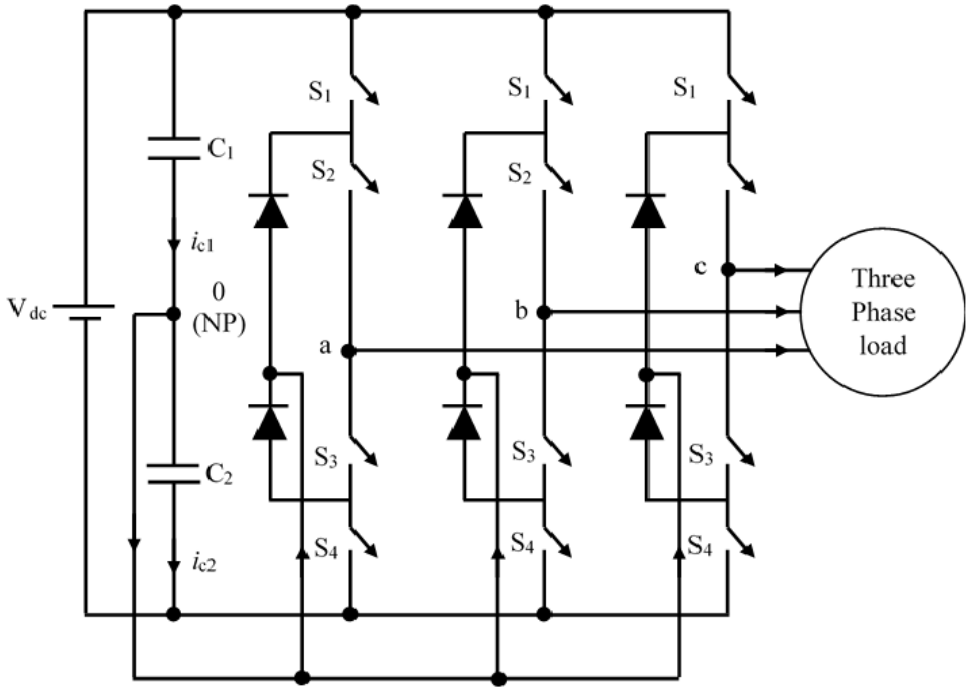

Figure 2.8 Schematic Diagram of Three Level Diode Clamped Inverter

2.5.2 Flying Capacitor Multilevel Inverter

The capacitor clamped type of the multilevel inverter is also called flying capacitor due to the fact that the capacitors in the circuit usually float with respect to the potential of the earth (Akhila *et al*., 2016). The flying capacitor multilevel inverter requires a large number of capacitors in order to clamp the device (switch) voltage to one capacitor voltage level. On condition that all the capacitors are of equal value, an n-level inverter according to Murugesan *et al*. (2016) will require a total number of (n-1)(n-2)/2 clamping capacitors per

phase leg in addition to (n-1) main dc bus capacitors. If the voltage of the main dc–link capacitor is V_{dc} , the voltage of innermost capacitor, the innermost two devices is V_{dc}/ (n-1). The voltage of the innermost capacitor will be V_{dc}/ (n-1) + V_{dc}/ (n-1) = 2V_{dc}/ (n-1) and so on. Each next clamping capacitor will have the voltage increment of V_{dc}/ (n-1) from its immediate inner single voltage level.

The advantage of this type of multilevel inverter is that phase redundancies are available for balancing the voltage levels of the capacitors, real and reactive power flows are controlled. The large number of capacitors enables the inverter to ride through short duration outages. The main disadvantages of this type of topology is that, it is very complicated to track the voltage levels for all of the capacitors. Also, the large number of capacitors needed are more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also difficult in inverters with a high number of levels (Murugesan *et al*., 2016). Figure 2.9 (Andrzej, 2016) shows the schematic diagram of three level flying (clamped) capacitor inverter.

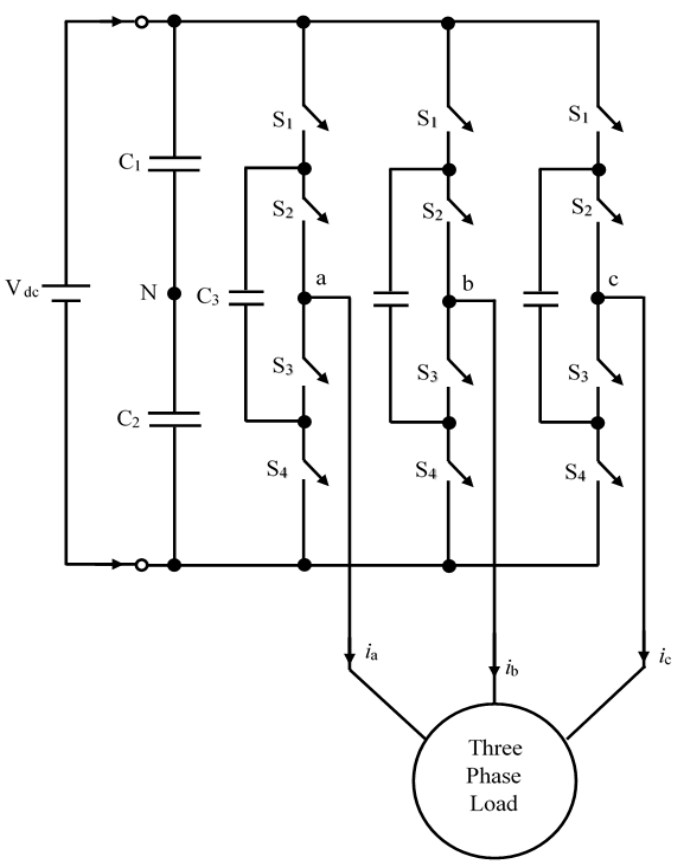

Figure 2.9 Schematic Diagram of Three Level Flying Capacitor Inverter

2.5.3 Cascaded H-Bridge Multilevel Inverter

The cascaded H-bridge multilevel inverter is based on addition of separate dc power supply voltages. In this type of multilevel inverter topology, each of the separate voltage sources (i.e. V_{dc1}, V_{dc2}, V_{dc3} ……) are connected in cascade with other sources through a special H-bridge circuit associated with it. The main advantage of this cascaded multilevel inverter is the series H-bridge for modularised layout and packaging (Boudaghi and Tousi, 2012). Also, it is cheaper in terms of cost. Its main disadvantage is that, it needs a separate dc source for each of the H-bridges. The use of solar battery or fuel cell where rectifiers and input transformers are employed is an example of such converters (Yuriy *et al*., 2016). Figure 2.10 (Murugesan *et al*., 2016) illustrates the schematic diagram of cascaded H-bridge multilevel inverter. The number of output voltage levels and number of switches can be calculated using Equation (2.6) and Equation (2.7) (Murugesan *et al*., 2016), respectively.

$$N_L = 2s + 1 \quad (2.6)$$

$$N_S = 4s \quad (2.7)$$

where; N_L = number of output voltage levels

N_S = number of switches

S = number of voltage sources

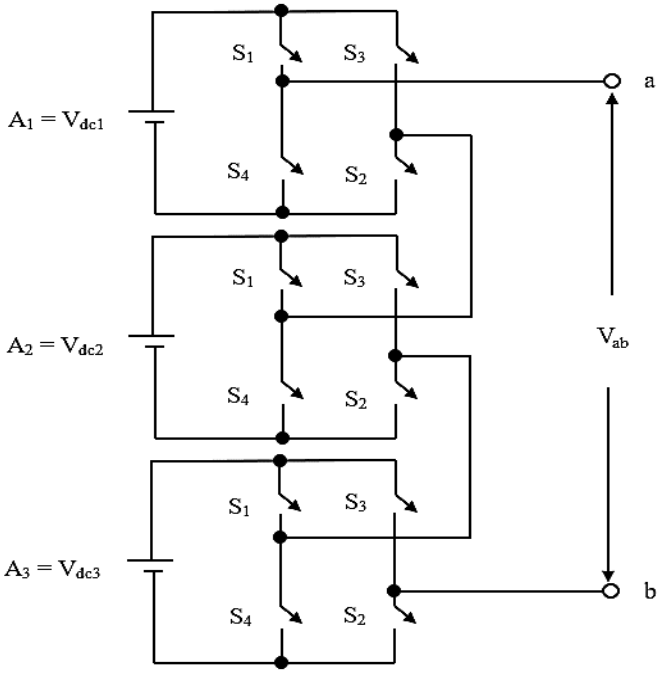

Figure 2.10 Schematic Diagram of Cascaded H-Bridge Multilevel Inverter

2.5.4 Hybrid H-Bridge Multilevel Inverter

The hybrid H-bridge multilevel inverter is similar to that of cascaded H-bridge multilevel inverter. The only difference between the two topologies is that it has a high number of levels with lesser number of bridges if compared to the cascaded H-bridge multilevel inverter. The main advantages of hybrid multilevel inverter is that, it has a high number of levels with reduced number of bridges and the dc sources are not of equal value. Figure 2.11 (Murugesan *et al*., 2016) illustrates the schematic diagram of hybrid H-bridge multilevel inverter. Its number of output voltage levels and number of switches can be calculated using Equation (2.8) (Murugesan *et al*., 2016).

$$N_L = 2^{s+1} - 1 \tag{2.8}$$

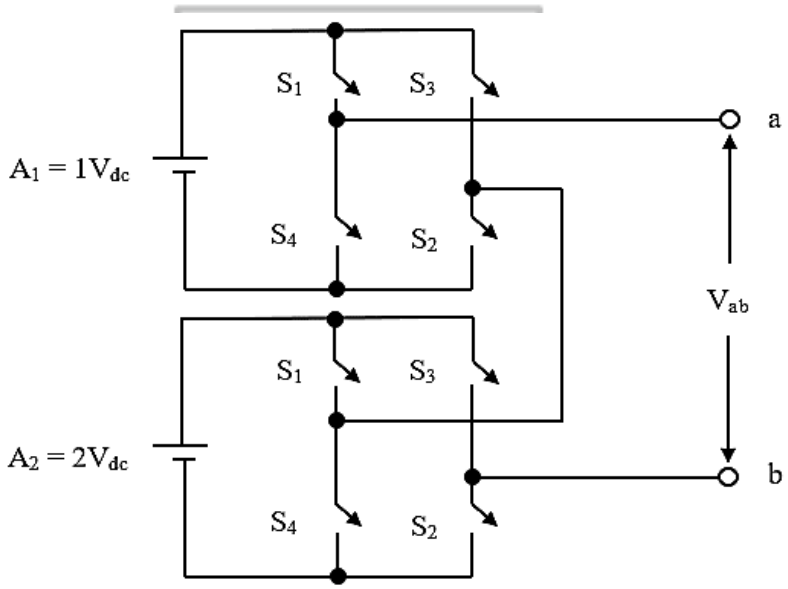

Figure 2.11 Schematic Diagram of Hybrid H-Bridge Multilevel Inverter

2.6 Custom Power Devices for Mitigation of Harmonics

A Custom Power Device (CPD) is the type of Flexible AC Transmission System (FACTS) controller that is mainly used in power distribution systems (Ambarnath *et al*., 2012), hence the name CPD. They are power electronic devices or static controllers used in power distribution systems that are rated from 1 kV to 38 kV with the aim of supplying certain levels of reliable power or the quality of power that is needed by electric power consumers

whose equipment are very sensitive to power variations (Devaraju *et al.*, 2010). The custom power devices are: Distribution Static Compensator (DSTATCOM) for compensating load reactive power and current harmonics; Dynamic Voltage Restorer (DVR) for compensating problems associated with voltage and Unified Power Quality Conditioner (UPQC) for both current and voltage compensation (Mani and Naidu, 2015).

2.6.1 Distribution Static Compensator

DSTATCOM is one of the custom power devices which is commonly used for mitigating current-based power quality problems, especially in power distribution systems (Bhim *et al.*, 2015). Shunt active power filter in current control mode is referred to as DSTATCOM. These shunt active power filters are used to mitigate harmonic currents in nonlinear loads. DSTATCOMs are basically classified into three types, namely, single-phase two wire, three-phase three wire, and three phase four wire configurations in order to meet the requirement of the various types of loads. DSTATCOM in general is used in power distribution systems to either generate or absorb reactive power depending on the problem concerned. DSTATCOM for mitigating harmonics in power distribution systems can also be classified based on the type of converter used.

The DSTATCOM is made up of coupling transformer with a leakage reactance, a three phase Insulated Gate Bipolar Transistor (IGBT) VSI and a DC capacitor. The DSTATCOM employs an inverter in order to convert the DC link voltage V_{dc} on the capacitor to a voltage source of adjustable magnitude and phase. Therefore, the D-STATCOM can be treated as a voltage controlled source. The DSTATCOM can also be seen as a current controlled source (Kishore and Reddy, 2014). The main function of the VSI is to produce a sinusoidal AC voltage with minimal harmonic distortion from a DC voltage. The principle of operation of the DSTATCOM is as follows: The voltage is compared with the AC bus voltage system (V_s). When the magnitude of AC bus voltage is above that of the VSI (V_c); the AC system sees the DSTATCOM as inductance connected to its terminals. Otherwise, if the VSI voltage magnitude is above that of the AC bus voltage magnitude, the AC system sees the DSTATCOM as capacitance to its terminals. If the voltage magnitudes are equal, the reactive power exchange is zero.

If the DSTATCOM has a DC source or energy storage device on its DC side, it can supply real power to the power system. This can be achieved by adjusting the phase angle of the DSTATCOM terminals and the phase angle of the AC power system. When phase angle of the AC power system leads the VSI phase angle, the DSTATCOM absorbs the real power from the AC system. If the phase angle of the AC power system lags the VSI phase angle, the DSTATCOM supplies real power to AC system. Figures 2.12 and 2.13 (Bhim *et al*., 2015) illustrate current source converter based DSTATCOM and voltage source converter based DSTATCOM, respectively. A diode is used in series with the IGBT self–commutating device for the reverse voltage blocking. The voltage source converter has self-supporting DC voltage bus with a large DC capacitor. It has the advantage of being expanded to a multiple level to enhance the performance with lower switching frequencies.

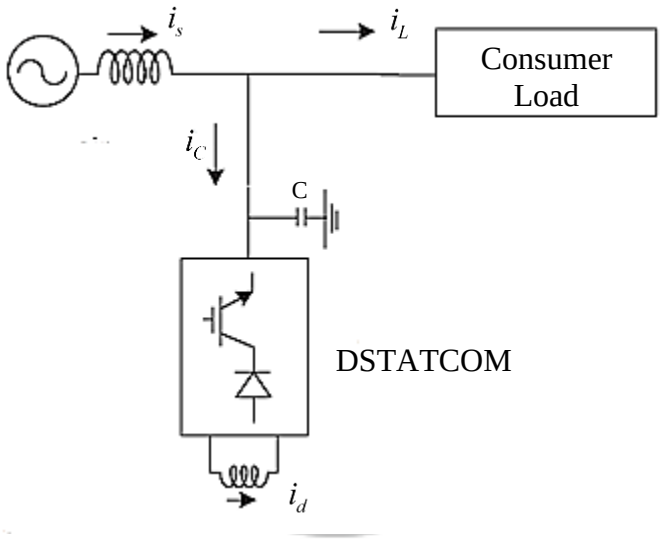

Figure 2.12 Current Source Converter–based DSTATCOM

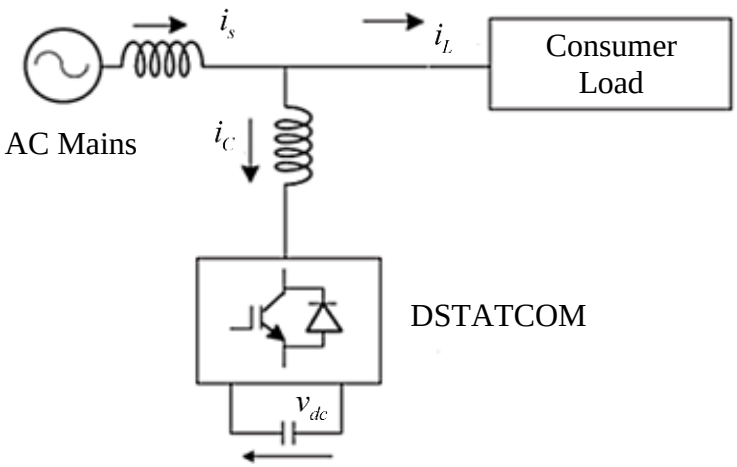

Figure 2.13 Voltage Source Converter-based DSTATCOM

2.6.2 Dynamic Voltage Restorer

Dynamic Voltage Restorer (DVR) is a custom power device mainly used in solving voltage related problems in power distribution systems and it is normally connected in series to the load (Mahmoud *et al*., 2013). The function of this device is to protect sensitive loads from experiencing voltage sag or swell, which is an interruption in the system. DVR is a fast, flexible and efficient solution for mitigating voltage sag and voltage swell problems (Vivek and Monika, 2016). DVR is a recent and very essential custom power device for compensation of voltage generated power quality problems in power distribution systems. Its main function is to quickly boost up the load-side voltage in the event of a voltage sag in order to avoid any power disruption to that load. Figure 2.14 (Shazly *et al*., 2013) illustrates the location of DVR in a power distribution network.

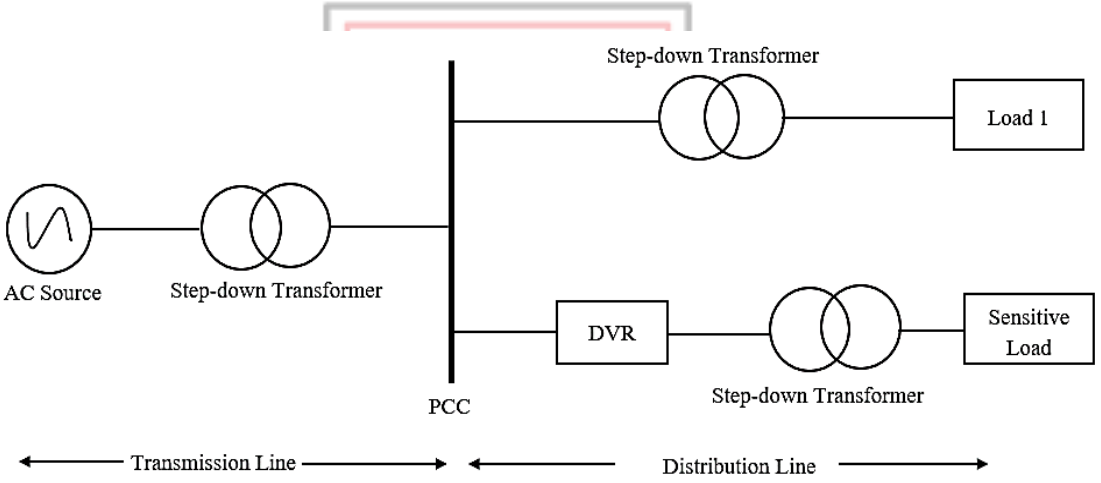

Figure 2.14 Location of a Dynamic Voltage Restorer

2.6.3 Unified Power Quality Controller

The Unified Power Quality Controller (UPQC) is a very versatile custom power device that can inject current in shunt circuit and voltage in series circuit simultaneously in a dual control mode. Therefore, it can perform the functions of both voltage and current based compensation, respectively (Pawar *et al*., 2016). Due to its versatility (compensating the unbalanced conditions of both voltage and current), fast response, nominal cost and high reliability amongst the custom power devices, it is generally considered as the best option for solving power quality problems in power distribution systems (Desale *et al*., 2014).

2.7 Proportional-Integral-Derivative Control

The design of a control system is about creating a dynamic system that can behave in a predetermined way in order to give a desired output. The controller modifies the behaviour of the system so that it can behave in a specific desirable way over a period of time. The aim of feedback control is to make sure that, the output of the plant, Y(s) follows the reference input R(s) as close as possible. The basic working principle of the Proportional-Integral-Derivative (PID) controller in a closed-loop system using the block diagram is shown in Figure 2.15. The variable e(s) represents the tracking error, that is, the difference between the desired input value R(s) and the actual output Y(s). This error signal serves as the input to the PID controller, and the controller computes its output signal U(s) based on the PID algorithm. For the PID controller, U(s) is expressed using Equation (2.9).

$$u = K_p e + K_i \int e dt + K_d \frac{de}{dt} \qquad (2.9)$$

where, K_p = proportional gain

K_i = integral gain

K_d = derivative gain

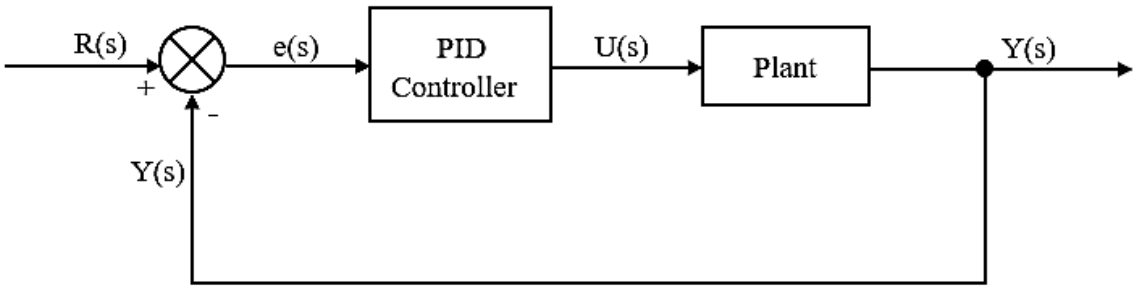

Figure 2.15 Block Diagram of Unity Feedback Control System

Proportional gain, K_p has the effect of reducing the rise time but will not eliminate the steady-state error. Integral gain, K_i has the effect of eliminating the steady-state error, but it may make the transient response worse. Derivative gain, K_d increases the stability of the system, reducing the overshoot, and improving the transient response. The effects of each gain parameter K_p, K_i and K_d on a closed-loop system are summarised into Table 2.1.

Table 2.1 Effect of PID Controller Gain Parameters on a Control System

SN	Gain Parameter	Rise Time	Overshoot	Settling Time	Steady State Error
1.	K_p	Decrease	Increase	Small Change	Decrease
2.	K_i	Decrease	Increase	Increase	Eliminate
3.	K_d	Small Change	Decrease	Decrease	Small Change

(Source: Tehrani and Mpanda, 2015)

2.8 Review of Related Works on the Mitigation of Harmonics in Power Distribution Systems

Geetha and Devi (2012) in their work focused on the control techniques employed for DSTATCOM. They considered VSC-based DSTATCOM employed in power distribution systems. They did comparison between phase shift control and AC/DC link voltage schemes which were incorporated to control the STATCOM. In conclusion, it was proposed that DSTATCOM's control scheme should be done such that, a complete reactive power compensation, power factor correction and voltage regulation of the harmonics can also be checked, in order to achieve improved power quality levels at the distribution end.

Malleswararao *et al*. (2015) investigated a five level cascaded H-bridge multilevel inverter-based DSTATCOM with fuzzy logic controller in 11 kV power distribution system for compensation of reactive power and harmonic mitigation. Cascaded H-bridge inverter was considered due to its advantages of reduced harmonic distortion and reduction in number of switches thereby reducing switching losses. In their investigation, d-q reference frame theory was used to generate reference compensating currents for the DSTATCOM whiles fuzzy logic controller was used for capacitor dc voltage regulation. In addition, Level Shifted Pulse Width Modulation (LSPWM) and Phase Shifted Pulse Width Modulation (PSPWM) techniques were implemented to analyse the performance of the cascaded H-bridge inverter. The source voltage, load voltage, source current, load current, power factor simulation results under nonlinear loads were investigated for LSPWM. From the tabulated results, it was concluded that fuzzy-based DSTATCOM controller is better than the PI controller techniques.

Mahesh *et al*. (2016) in their investigation considered multilevel inverter as DSTATCOM for harmonic compensation. A shunt active power filter as cascaded H-bridge multilevel

inverter DSTATCOM with phase shifted PWM technique was proposed to mitigate harmonic components in the source currents. The mathematical modelling of the system and the controller design were done using Synchronous Reference Frame (SRF) theory. Their results showed that, the cascaded H-bridge multilevel inverter and DSTATCOM have the advantage of mitigating harmonics in the source current of power distribution system to meet IEEE 519–1992 standards.

Srikanth (2013) presented a modified SRF method for real time generation of compensating current for harmonic mitigation, active and reactive power compensation. He proposed a fast-acting DC-link voltage controller based on the energy of the dc-link capacitor. A comparison between conventional and fast acting DC-link voltage controller for improving the transient performance of the compensator for nonlinear and unbalanced loads to improve power quality was then carried out. By the use of fast-acting DC-link voltage controller, harmonic filtering, voltage regulation, load balancing and unity power factor were all achieved.

Kalyani and Kamaraju (2015) proposed a scheme for new multilevel state-space model-based DSTATCOM together with a deadbeat prediction controller and five-level cascaded multilevel inverter to solve the problem of harmonic mitigation of nonlinear loads in distribution systems. PI controller was used to regulate the dc capacitor voltage at a reference value. The use of cascaded multilevel H-bridge inverter for DSTATCOM helped to decrease the output harmonics by increasing the number of output voltage levels of the device.

Babu and Elangovan (2017) proposed a five level cascaded H-bridge multilevel inverter-based DSTATCOM with the use of multi-carrier PWM technique and SRF theory to regulate the output voltage and to reduce THD. They created a very smooth stepped output waveform by combining more than two voltage levels together and the output waveform obtained in this case has lower dv/dt and also lower harmonic distortions. Smoothness of the output waveform was found to be proportional to the voltage levels, thus, an increase in voltage level results in the smoothness of the waveform. SRF control technique was used to generate gate pulses for control of the DSTATCOM. The cascaded H-bridge multilevel inverter-based DSTATCOM was effective in harmonic mitigation compared to a diode clamped multilevel inverter-based DSTATCOM.

Kayasth and Hasabe (2017) investigated the compensation of reactive power and harmonics in power distribution systems by using cascaded H-bridge multilevel inverter based DSTATCOM with five level voltage output. The rotating SRF theory was used in generating the reference compensating current for DSTATCOM. The capacitor DC link voltage of H-bridge was regulated using PI controller. The cascaded H-bridge inverter performance was carried out by level shifting PWM and phase shifting PWM techniques. It was found out that the multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of levels of output voltage waveform.

Chavan and Mahagaonkar (2015) investigated a multilevel cascaded H-bridge inverter-based DSTATCOM for mitigation of harmonics and compensation of reactive power. PI controller was used in regulating the capacitor dc voltage whiles level shifted PWM was used to analyse the performance of the inverter. They concluded that using multilevel converters will not only eliminate just a specific harmonics but rather minimise the THD.

Benazir *et al*. (2014) investigated the use of SRF theory (i. e. d-q theory) in the extraction of compensated reference current and the use of fuzzy logic controller in reducing load current harmonics. The triggering of the gate pulse was achieved by using PWM controller on a three phase shunt active filter. They concluded that fuzzy logic controller compared to the conventional PI controller has a better dynamic performance in compensating current harmonics in a 3-phase, 4-wire system. Also, use of SRF theory (i_d-i_q) for obtaining the reference currents in the system avoids the large number of synchronisation problems.

Mahdianpoor *et al*. (2017) proposed use of proportional resonant controller for DSTATCOM performance improvement since the conventional PI controller has the drawback of steady state error when used in stationary frame. They maintained that to improve the DSTATCOM structure, an LCL harmonic filter should be used since it has many advantages over the conventional filters. The proportional resonant controller when used in abc-frame helped in load balancing and harmonic suppression.

Adarsh and Sijo (2015) investigated two methods of reference current generation by comparing instantaneous reactive power theory and SRF theory. Hysteresis PWM control and Sinusoidal PWM used to control the switching pulses for the inverter were also compared. Conventional PI controller was used in DC link voltage regulation. From their

investigations, it was concluded that conventional controls like instantaneous reactive power theory also known as PQ theory and SRF can be used for harmonic mitigation in power distribution systems. That the two control methods provide compensation at a satisfactory level, but SRF control in combination with hysteresis PWM current control provides better compensation to the system in terms of harmonics and THD.

Hurkadli and Kulkarni (2017) in a research suggested that regarding current control techniques, the most significant part of the DSTATCOM is the generation of switching signals. They stated that the most effective way of getting the desired output voltage waveform is by the use of PWM. In order to achieve the desired signal, the frequency of the switching signal should be significantly higher than that of the desired signal.

Mokhtari *et al*. (2014) described PI controller as the most common industrial technique used when selecting or designing controllers for DSTATCOM achievable by a judicious choice of the PI parameters.

Hinduja *et al*. (2015) proposed a five-level cascaded multilevel inverter based shunt active power filter for the compensation of reactive power and the mitigation of harmonic currents generated by the nonlinear loads. They considered the use of PI controller for dc link voltage regulation and triangular carrier current controller for the generation of switching pulses for the inverter switches. SRF theory was used as the control strategy for extracting the harmonic components from distorted line currents which in turn are utilised in the production of required reference compensation currents. The control strategy for reference current extraction based on SRF theory provided a better extraction of reference compensation currents from the distorted line current.

2.9 Summary

In the literature, DSTATCOM with different control techniques for effective performance were reported. Among the inverters, multilevel VSI was recommended due to its advantages of reduced harmonic distortion and reduced voltage steps (dv/dt) thereby reducing switching losses as compared with two level VSI. Mostly considered in the literature is the multilevel inverter based DSTATCOM with five level voltage output for a 3-phase 4-wire system. The use of SRF theory, Instantaneous Reactive Power (IRP) theory, fuzzy logic controller, PI

controller and several other methods for generating compensating current and control techniques for both voltage and current controls were considered and reported. PWM technique was proposed for generating the gate pulses for the semiconductor device.

From research conducted, the return of current harmonics generated by the nonlinear load to the source of supply leads to voltage harmonics. These voltage harmonics affect the entire power distribution system and not just the load causing it. From the literature, different approaches were used for the harmonic reduction. Therefore, this research work focuses on mitigating harmonics in the source current using three level Neutral Point Clamped (NPC) multilevel inverter-based DSTATCOM with SRF theory and PI controller techniques.

CHAPTER 3

METHODOLOGY

3.1 Introduction

This section of the thesis discusses the methods used in the research. The specific areas considered are: the description of the main circuit arrangement and the functions of the various components that are employed in the design. In the modelling of the power distribution system, a stiff power source with 50 kVA, 400 V, 50 Hz, was considered. These values are the ratings of a distribution transformer used by PDS. The simulation and analysis were done using MATLAB/Simulink software environment.

3.2 General Description of the Proposed System

In the basic structure of the system both linear and nonlinear loads were connected to the three phase three wire distribution system with a stiff power source. The linear load was realised by connecting resistance and inductance (R-L) as a load. The nonlinear load is then connected as diode bridge with resistance and inductance (R-L) as a load. The simplest circuit to represent a non-linear load is a diode-rectifier (Ramon, 2015). The DSTATCOM is then connected as shunt compensator which is designed with three level neutral point clamped voltage source inverter with the dc capacitor voltage as its input. A control technique is used to control the gating signal to the voltage source inverter based DSTATCOM. The AC voltage output from the inverter is supplied to the distribution system through the interface RL filter. In this arrangement, PI controller was used for voltage control. The main function of this PI controller is to control the DC voltage, V_{dc} stored in the capacitor, C_{dc} in order to maintain a constant DC voltage for a perfect current tracking.

The switching of the DSTATCOM is achieved by reference currents which the real fundamental frequency of the load current, where another two PI controllers were used for current (inner) control. In the three-level diode clamped multilevel inverter based DSTATCOM as proposed, Synchronous Reference Frame (SRF) theory was used for the reference current generation. The SRF control has been noted as one of the effective controls, to be used for current extraction when mitigating current harmonics (Peeriah and

Rao, 2017). The point at which the DSTATCOM is connected is referred to as the utility customer Point of Common Coupling (PCC). A three winding transformer with turn's ratio of 1:1:1, was used as PCC. Figure 3.1 shows the block diagram of the propoed system. During the simulations using MATLAB software, circuit breakers were also used to determine the on and off connections of the connected loads.

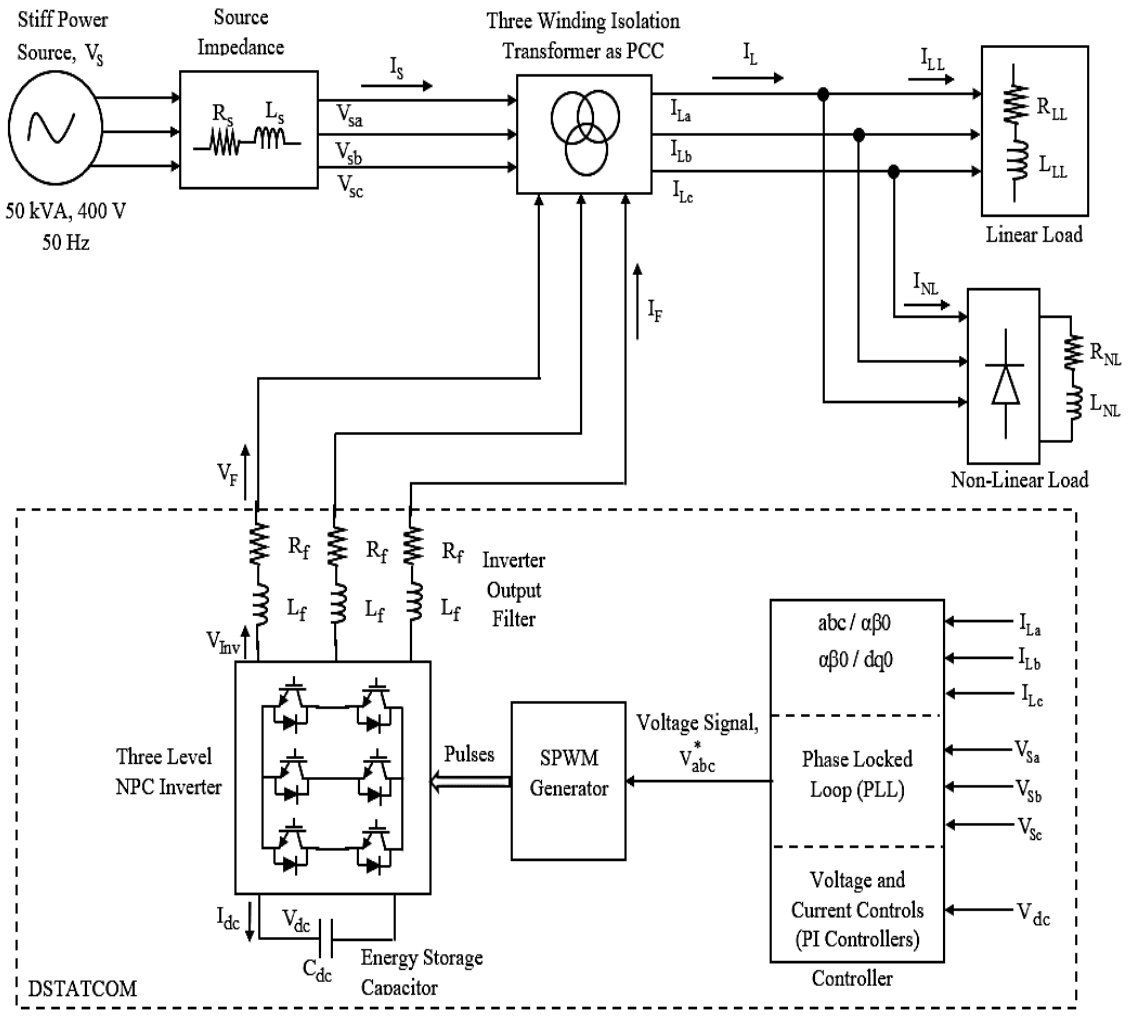

Figure 3.1 Block Diagram of the Proposed System

3.3 The AC Voltage Source

The stiff power source as shown in Figure 3.1, is a three phase AC voltage source having a magnitude of V_S with the frequency of 50 Hz. It is referred to as a stiff power source because there is no significant feeder impedance between the load and the source aside of the internal impedance. Each of the voltage phase vectors is given in Equations (3.1), (3.2) and (3.3), respectively.

$$V_{sa} = V_s \sin(\omega t + \phi) \tag{3.1}$$

$$V_{sb} = V_s \sin\left(\omega t + \phi - \frac{2\pi}{3}\right) \tag{3.2}$$

$$V_{sc} = V_s \sin\left(\omega t + \phi + \frac{2\pi}{3}\right) \tag{3.3}$$

where, V_{sa}, V_{sb}, V_{sc} = phase vectors in volts

V_s = source voltage in volts

ω = angular frequency of the waveform in radian/sec.

ϕ = phase difference (angle) in radian

The source impedance is therefore given as in Equation (3.4).

$$Z_s = R_s + jX_s \tag{3.4}$$

where, Z_s = source impedance in ohms

R_s = source resistance in ohms

L_s = source inductance in ohms

Due to the presence of source impedance, there will be a drop in the voltage available at the PCC due to which the voltage to the loads will also drop to V_o . The expression for V_o is given by Equation (3.5).

$$V_o = V_s - V_d \tag{3.5}$$

where, V_o = voltage available to the load in volts

V_d = voltage drop in volts

The voltage drop across the source impedance depends on two terms normally referred to as resistive and inductive drops as given in Equations (3.6) and (3.7), respectively.

$$V_R = i_s \times R_s \tag{3.6}$$

$$V_L = L_s \times (di_s/dt) \tag{3.7}$$

where, i_s = source current in amperes

L_s = source inductance in henry

Therefore, Equations (3.8), (3.9) and (3.10) represent the phase voltages.

$$V_a = V_{sa} - (i_s R_s) - L_a (di_a/dt) \quad (3.8)$$

$$V_b = V_{sb} - (i_s R_s) - L_b (di_b/dt) \quad (3.9)$$

$$V_c = V_{sc} - (i_s R_s) - L_c (di_c/dt) \quad (3.10)$$

where, V_a, V_b, V_c = phase voltages in volts

L_a, L_b, L_c = phase inductances in henry

i_a, i_b, i_c = phase currents in amperes

3.4 The Three Winding Isolation Transformer

Three winding transformer is a type of transformer which is made up of three separate windings namely, primary, secondary and tertiary windings. In its normal construction, the voltage ratings of all the three windings of the transformer are usually unequal. The primary winding has the highest voltage rating; the tertiary has the lowest voltage rating; and the secondary has the intermediate voltage rating. But in this research, the three winding transformer is being used as an isolation transformer to create the utility PCC.

In general, the isolation transformer is a device used to decouple two circuits, thus the load to the isolation transformer and the supply input. In other words, its function is to isolate the load and the DSTATCOM from the distribution network. Isolation transformer is capable of blocking the transmission of DC signals from one circuit to the other and allow only ac signals to be transmitted. There is no voltage change of an isolating transformer because the primary and secondary windings have the same number of turns. Isolation transformer in general has a unity transformation ratio which is 1:1:1. Due to the constructional features of an isolation transformer, its leakage reactance is able to offer some level of circuit impedance which helps in attenuating the harmonic content. In other words, isolation transformer keep harmonics produced by customers through the use of nonlinear load from

getting onto the utilities systems. In this research, a three winding transformer is used as an isolation transformer by maintaining the same value of voltages across the three windings. With the power supply source connected to the primary winding, the load is connected to the secondary whiles the VSI-based DSTATCOM is connected to the tertiary winding. Figure 3.2 illustrates the circuit diagram of a three winding transformer.

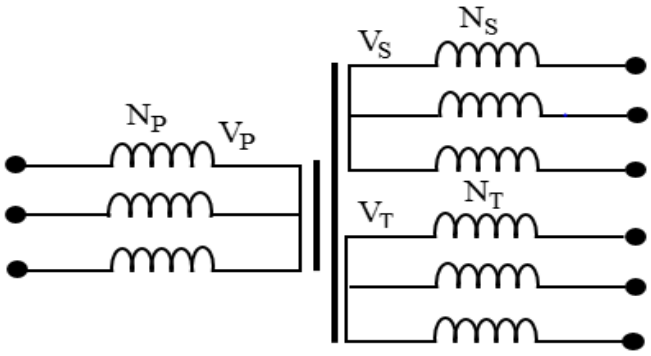

Figure 3.2 Circuit Diagram of a Three Winding Transformer

$$\frac{V_P}{N_P} = \frac{V_S}{N_S} = \frac{V_T}{N_T} \tag{3.11}$$

$$N_P i_P = N_S i_S = N_T i_T \tag{3.12}$$

where, V_P, V_S, V_T = primary, secondary and tertiary voltages in volts

N_P, N_S, N_T = primary, secondary and tertiary number of turns

i_P, i_S, i_T = primary, secondary and tertiary currents in amperes

3.5 Resistive – Inductive Load and the Rectifier

Whenever there is the need to raise the reactive power demanded by the load, then the load must be designed as a star connected unbalanced load (Prasad and Sudhakar, 2017). The R–L load is not a pure resistive load. The reactive power demand in this case causes disturbances in the voltage profile of the system. This at the end necessitated the use of DSTATCOM on the system in order to provide compensation so that a constant voltage can be maintained. In this thesis report, the attention is on harmonics reduction in the system. As widely known, rectifier is the device which converts AC voltage or current to DC. In this arrangement, the bridge rectifier converts three phase AC to DC. The DC side of the rectifier

is connected with an R–L load with resistance, R_d and inductance, L_d. Since the operation of the rectifier involves power electronic switching, it acts as a nonlinear load by injecting harmonics into the system which normally leads to distortion of the supply current waveform. This has to be mitigated therefore, the DSTATCOM is connected to PCC for compensation. Each of the phase currents drawn by the (linear load) R–L can be calculated through the differential equations as given in Equation (3.13), Equation (3.14) and Equation (3.15), respectively.

$$\frac{di_a}{dt} = \frac{1}{L_{La}}\left(-i_a R_{La} + V_a\right) \tag{3.13}$$

$$\frac{di_b}{dt} = \frac{1}{L_{Lb}}\left(-i_b R_{Lb} + V_b\right) \tag{3.14}$$

$$\frac{di_c}{dt} = \frac{1}{L_{Lc}}\left(-i_c R_{Lc} + V_c\right) \tag{3.15}$$

where, R_{La}, R_{Lb}, R_{Lc} = load resistance per phase in ohms

L_{La}, L_{Lb}, L_{Lc} = load inductance per phase in ohms

The current at the AC side of the rectifier is of great importance, as it is considered as the total AC load current drawn. The DC current drawn by the DC side of the rectifier is taken as I_{dc}. The total AC current drawn by the load can be calculated as the sum of rectifier current and R–L load currents which are given in Equation (3.16), Equation (3.17) and Equation (3.18).

$$i_r = i_{ra} + i_{rb} + i_{rc} \tag{3.16}$$

$$I = I_a + I_b + I_c \tag{3.17}$$

$$i_t = i_r + I \tag{3.18}$$

where, I_{ra}, I_{rb}, I_{rc} = current drawn by the rectifier per phase in amperes

I_r = current drawn by the rectifier

I = current drawn by the R–L load in amperes

i_t = total AC current drawn by both rectifier and R–L load in amperes

The current, I_t contains the harmonics due to the nonlinear nature of the load where this current is to be compensated using the DSTATCOM.

3.6 Distribution Static Compensator

In this thesis report, the DSTATCOM is made up of an inverter which is a three level Voltage Source Inverter (VSI), hence the name VSI-based DSTATCOM. The VSI performs the function of producing the required voltage and current. The three winding isolation transformer serves as the PCC where the load and the DSTATCOM are connected to the supply. DC link capacitor acts as the energy storage device which provides the dc source voltage for the inverter. The main function of the current control unit in the structure is to develop switching pulses of the inverter from the required output waveforms that are given to the PWM. When the inverter takes the dc voltage, V_{dc} from the energy storage device, the PWM therefore, sends a switching signal to the inverter which enables the inverter to generate the desired output voltage, V_F and current, i_F. In this case, the on and off mode of the switches are commanded by PWM. In order to generate the switching pulses, first the magnitude of various voltages and currents will be considered and then given to the controller of DSTATCOM for comparison.

In this thesis work, the controller uses Synchronous Reference Frame (SRF) theory as the control algorithm for the extraction of reference currents. The magnitude of current after the controller execution results into the switching signal of the inverter through the PWM. In the end, the switching devices of the inverter get activated for generating the sinusoidal ac current output. The controller is basically divided into two parts, namely voltage control and current control. Figure 3.3 depicts the block diagram of the DSTATCOM.

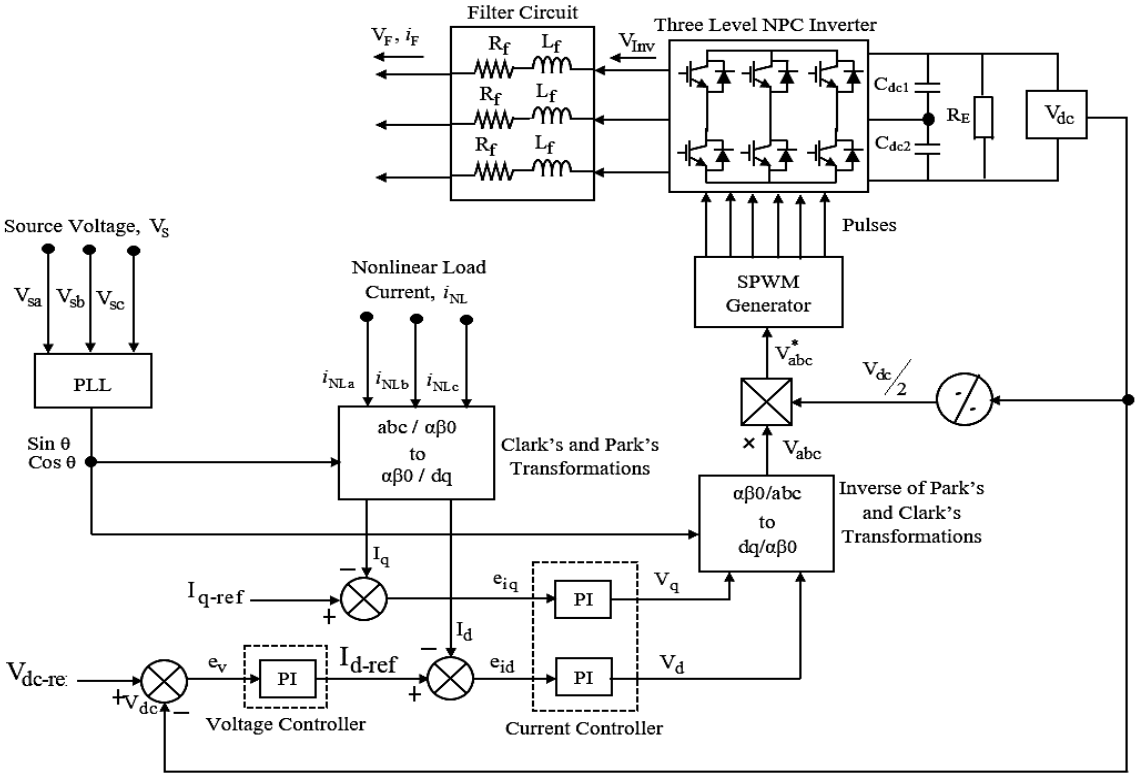

Figure 3.3 Block Diagram of the Structure of DSTATCOM

3.6.1 Operating Principle of DSTATCOM

The VSI-based DSTATCOM acts as a current source that compensates the harmonic currents due to the nonlinear load. The DSTATCOM operation is based on the injection of compensation current which is equal to the distorted current, thus eliminating the original distorted current. This is achieved by shaping the compensating current waveform (i_F) using the VSI switches. The shape of the compensation current is obtained by measuring the nonlinear load current, i_{NL} and subtracting it from the sinusoidal reference current, i_S.

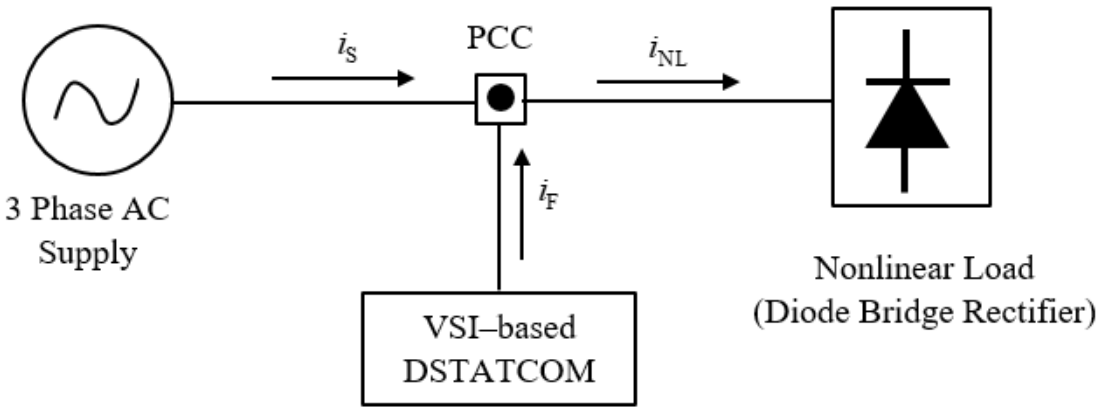

Figure 3.4 Simplified Configuration of VSI-based DSTATCOM

Figure 3.4 illustrates a simplified block diagram of the configuration of the VSI-based DSTATCOM to the network. Applying Kirchhoff's current law at the PCC of Figure 3.4, the sinusoidal source current can be obtained using the expression as given in Equation (3.19).

$$i_S = i_{NL} - i_F \tag{3.19}$$

where, i_{NL} = nonlinear load current in amperes

i_F = filtered injected VSI current in amperes

Assuming that the nonlinear load current can be written as the sum of the fundamental current component ($i_{NL,f}$) and the harmonic current ($i_{NL,h}$), then, the expression for the nonlinear load current is as given in Equation (3.20).

$$i_{NL} = i_{NL,f} + i_{NL,h} \tag{3.20}$$

where, $i_{NL,f}$ = nonlinear load fundamental current in amperes

$i_{NL,h}$ = nonlinear load harmonic current in amperes

Therefore, the injected compensating current is obtained as shown in Equation (3.21).

$$i_F = i_{NL,h} \tag{3.21}$$

The resulting source current can now be obtained by the expression given in Equation (3.22).

$$i_S = i_{NL} - i_F = i_{NL,f} \tag{3.22}$$

This source current now contains only the fundamental component of the nonlinear load current and hence free from harmonics.

3.6.2 Synchronous Reference Frame Theory

SRF theory is the most commonly used control algorithm for the extraction of reference currents in DSTATCOM (Gupta and Chaudhari, 2015). This method is often used based on the study of calculation of the desired signals with respect to time. The SRF theory mainly focuses on the determination of reference currents from the affected load current signals where DSTATCOM is to be used in the power distribution system in order to compensate for the harmonic current. This theory works on the principle of Park's transformation meaning conversion of three phase stationary current or voltage into two similar revolving components. In SRF theory, the conversion of the three phase stationary components is in the form of direct axis and quadrature axis which is also known as d-q theory. SRF theory acts like a harmonic current extractor. For the use of this method, three steps are usually taken for the measurement of reference currents and achievement of compensator currents by involving both Clark's and Park's transformations. Clark's transformation refers to the conversion of the components into $\alpha - \beta$ structure while Park's transformation is the d – q rotating structure. This is because signals in d-q frame are easy to control and be processed (Pathan *et al*., 2014). Finally, reverse conversion for Park's and Clark's transformations is done to achieve reference source currents as well as compensating currents. Figure 3.5 (Chandra, 2008; Desai *et al*., 2017) shows the phasor diagram of d-q transformation.

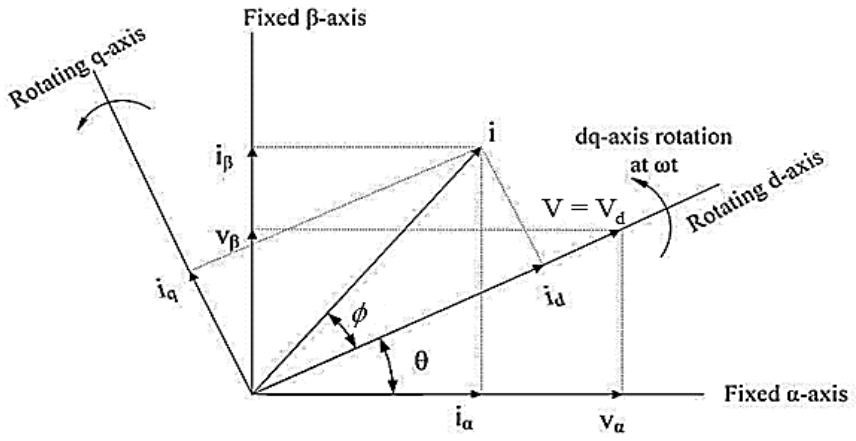

Figure 3.5 Phasor Diagram of D-Q Transformation

The Clark and Inverse-Clark transformations are used to convert the variables (e.g. phase values of voltages and currents) into stationary α-β reference frame and vice-versa. Similarly, Park and Inverse-Park transformations convert the values from stationary α-β

reference frame to synchronously rotating d-q reference frame, and vice versa. The control stages with the respective reference frames and transformations are shown in Figure 3.6 (Chandra, 2008; Desai *et al*., 2017).

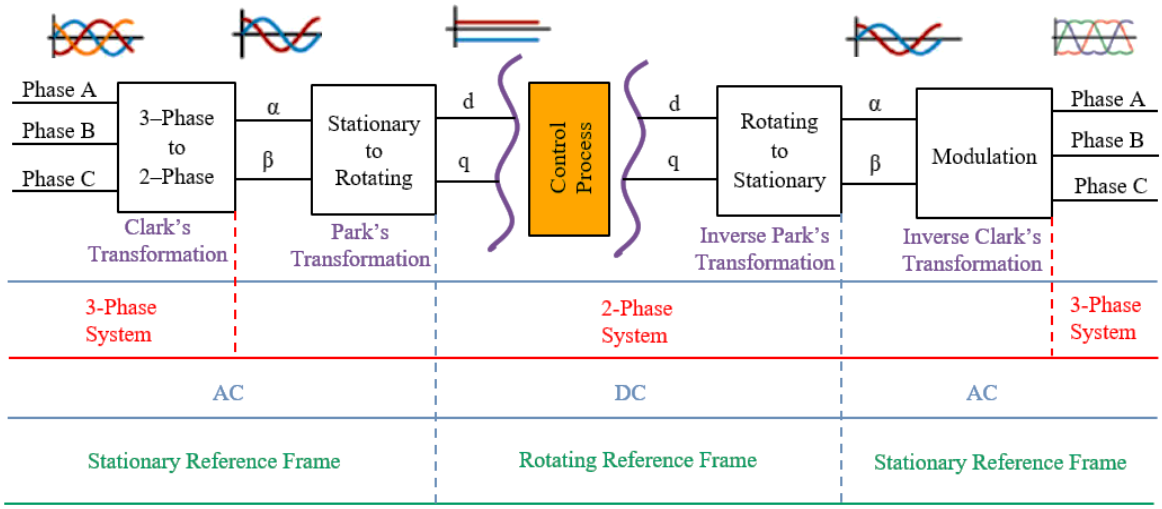

Figure 3.6 Control Stages and Respective Reference Frame

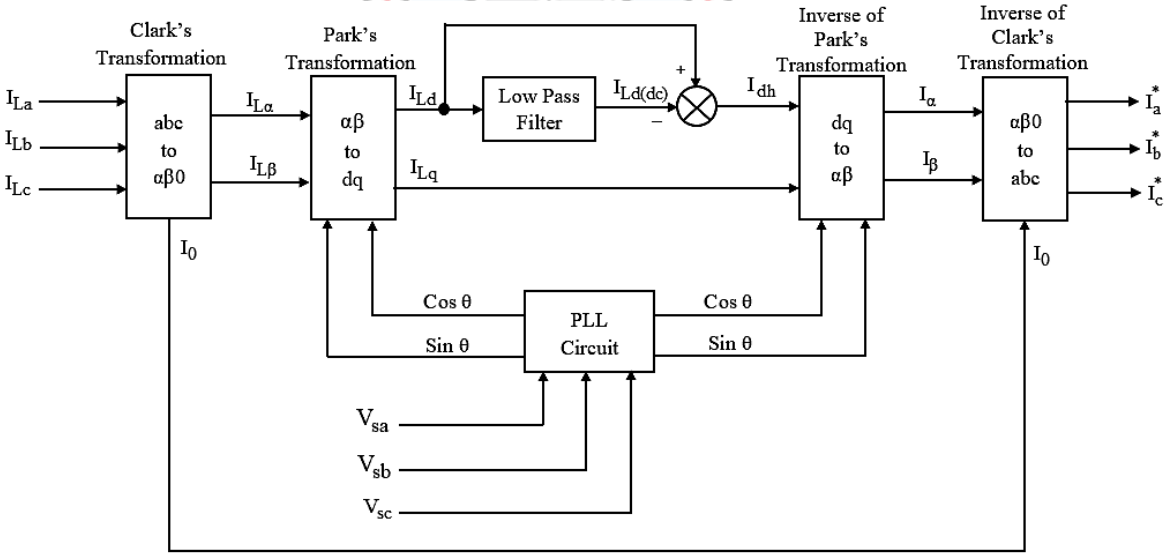

Figure 3.7 Block Diagram of Synchronous Reference Frame based Reference Current Extraction

From Figure 3.7, Phase Locked Loop (PLL) block is used in its control circuit on the three phase terminal voltages of the system, which are V_{sa}, V_{sb} and V_{sc}. The purpose of PLL is to develop sine and cosine angles while doing transformation based on Park's as well as

reverse conversion of Park's and Clark's methods. PLL is incorporated for producing angles in the conversion blocks. Three phase load currents which are in a, b, c components are first converted into two phase components in $\alpha-\beta$ structure based on Clark's transformation. Figure 3.7 (Modified after Rejil *et al*., 2013) shows the block diagram of SRF method of reference current extraction.

From Figure 3.7, the load currents (i_{La}, i_{Lb}, i_{Lc}) are first detected at PCC and then transformed into two-phase stationary frame ($\alpha\beta0$) as $i_{L\alpha}$ and $i_{L\beta}$ from the three-phase stationary frame (abc). The transformation of the load current is as given in Equation (3.23).

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (3.23)$$

where, $i_{L\alpha}, i_{L\beta}, i_0$ = phase currents in two phase stationary frame ($\alpha\beta0$) in amperes

i_{La}, i_{Lb}, i_{Lc} = phase quantities of the three phase load current in amperes

Now, the stationary structure of $\alpha\beta$-axes of the two phase current quantities $i_{L\alpha}$ and $i_{L\beta}$ are transformed into two phase synchronous frame (dq–axes) also known as Park's transformation. The transformation of $\alpha\beta$ into dq is given in Equation (3.24), where $\cos\theta$ and $\sin\theta$ represent the synchronous unit vectors which usually are generated using PLL.

$$\begin{bmatrix} I_{Ld} \\ I_{Lq} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \quad (3.24)$$

where, I_{Ld}, I_{Lq} = phase currents in two phase synchronous frame (dq0) in amperes

θ = angle of transformation in rad/s (or degrees)

After the conversion of components from $\alpha\beta$ into the dq structure, the dq currents obtained comprise both AC and DC quantities as given in Equation (3.25). In this case, the DC part represents the fundamental component of current while the AC part represents the harmonic component.

$$\begin{bmatrix} I_{Ld} \\ I_{Lq} \end{bmatrix} = \begin{bmatrix} I_{Ld(dc)} + I_{Ld(ac)} \\ I_{Lq(dc)} + I_{Lq(ac)} \end{bmatrix} \tag{3.25}$$

where, $I_{Ld(dc)}$, $I_{Lq(dc)}$ = DC components in two phase synchronous frame in amperes

$I_{Ld(ac)}$, $I_{Lq(ac)}$ = AC components in two phase synchronous frame in amperes

The harmonic part can be extracted using the Low Pass Filter (LPF) indicated in Figure 3.7. The LPF is commonly used to separate the fundamental components from the harmonic component (Yap *et al.*, 2017). The d-axis current is made up of both active fundamental current ($I_{d(dc)}$) and the load harmonic current (I_h). The DC component is the fundamental component of current which rotates in synchronism with the rotating frame. Therefore, the current obtained after filtering I_d will be the fundamental component of the load current in the synchronous frame. In order to obtain the AC component, I_{dh}, the $I_{d(dc)}$ is subtracted from the total d-axis currents I_d leaving behind only the harmonic component present in the load current. The q-axis current (I_q) represents the fundamental reactive load currents and part of the load current. The inverse transformation is also performed in order to transform the currents from two phase synchronous frame (dq) into two phase stationary frame ($\alpha\beta$) as given in Equation (3.26).

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} I_{dh} \\ I_{Lq} \end{bmatrix} \tag{3.26}$$

where, I_{dh} = harmonic component in the load current of the d-axis in amperes

Finally, the current in the two phase stationary frame $\alpha\beta0$ is transformed back into the three phase stationary frame abc as given in Equation (3.27).

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \quad (3.27)$$

where, i_a^*, i_b^*, i_c^* = three phase stationary frame compensation reference currents in amperes

In this model, the two current controllers transform the error obtained after the comparison of d and q components of current into voltage values.

3.6.3 The Phase Locked Loop

The PLL is considered as a very important element when designing controllers for the DSTATCOM. It is based on Clark's transformation technique. The PLL block in this thesis work takes the source voltage signal, V_s and generates a synchronisation angle/phase (θ), so that inverter current, i_F which is injected by the DSTATCOM into the operating power system is correctly synchronised with the source voltage. The PLL can also help by providing information about the frequency of the system. In this work however, the main focus is on the generation of the transformation angle, θ. In order to transfer the variables from the abc frame to the synchronous reference frame (qd0), the transformation angle ($\theta = \omega t$) is required. This transformation angle, θ can be defined as the angle between the $\alpha\beta$ - frame and the qd0 - frame. Therefore, if the voltage vector as given in Equation (3.28) is defined in parallel with the q-axis in the qd0 - frame, then, the transformation angle, θ can be determined as given in Equation (3.29) and Equation (3.30). The magnitude of the voltage, V_o can be determined using Equation (3.31).

$$\vec{V_o} = \vec{V}_\alpha + j\vec{V}_\beta \quad (3.28)$$

$$\sin\theta = \frac{V_\alpha}{V_o} \quad (3.29)$$

$$\cos\theta = -\frac{V_\beta}{V_o} \quad (3.30)$$

$$V_o = \sqrt{V_\alpha^2 + V_\beta^2} \tag{3.31}$$

where, $\vec{V}_o$ = voltage vector in volts

$\vec{V}_\alpha$, $\vec{V}_\beta$ = vectors of phase voltages in two phase stationary frame ($\alpha\beta 0$) in volts

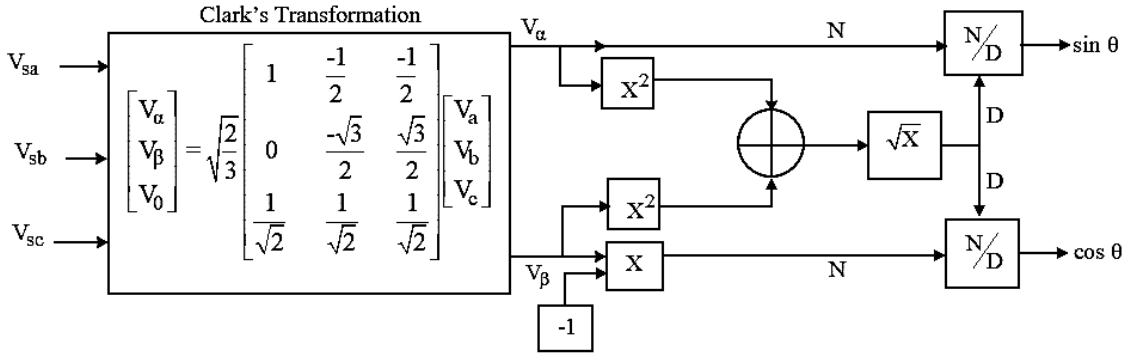

Figure 3.8 Block Diagram of the Phase Locked Loop

To get the transformation angle, the PLL is mathematically obtained in the MATLAB software. The three-phase instantaneous voltages are denoted by V_{sa}, V_{sb}, and V_{sc}. The corresponding voltages are transformed into $\alpha\beta$-frame and are denoted by V_α and V_β. Figure 3.8 shows the detailed block diagram of the PLL.

3.6.4 Three Level Neutral Point Clamped Voltage Source Inverter

In simple terms, an inverter which creates an AC voltage (and current) from a dc voltage source is termed as VSI. A VSI is a power converter which is systematically controlled to reproduce a reference current, I_{ref} as inverter current, i_F at its output at suitable magnitude. It is equipped with a DC-link capacitor (energy storage element) which also serves as input to the inverter. The fundamental AC voltage rating of the inverter was determined using Equation (3.32) (Bhim *et al*., 2015). The main function of the VSI is to produce a sinusoidal AC voltage at its output with minimal harmonic distortion from a DC voltage source, V_{dc} which serves as an input voltage to it.

$$V_{ac(rms)} = \frac{m_i V_{dc}}{2\sqrt{2}} \tag{3.32}$$

where, $V_{ac(rms)}$ = rms AC voltage in volts

m_i = modulation index

V_{dc} = DC source input voltage of the VSI in volts

The Neutral Point Clamped (NPC) multilevel inverter in its classification, uses capacitors in series to divide up the dc bus voltages into a set of voltage levels. In this model, the three level NPC multilevel inverter is controlled to produce the staircase voltage of three levels and sinusoidal current waveform. The circuit diagram of the three level NPC inverter is as shown in Figure 3.9. The voltages across each of the DC capacitors C_{dc1} and C_{dc2} are equal to half of the input DC voltage. The principle of operation of the circuit by considering only one arm (e.g., phase a) can be described as follows:

State 1: If the two upper transistors S_{a1} and S_{a2} are in the ON position, then the lower transistors S_{a3} and S_{a4} will be in the OFF position. This gives a voltage output of $V_{dc}/2$.

State 2: If transistors S_{a1} and S_{a4} are in the OFF position, then transistors S_{a2} and S_{a3} will be in the ON position. This gives a voltage output of '0'.

State 3: If the two lower transistors S_{a3} and S_{a4} are in the ON position, then the upper transistors S_{a1} and S_{a2} will be in the OFF position. This gives a voltage output of $-V_{dc}/2$.

Table 3.1 shows the switching state of the three level NPC inverter considering only phase A. The state condition 1 means switch is ON and 0 means switch is OFF.

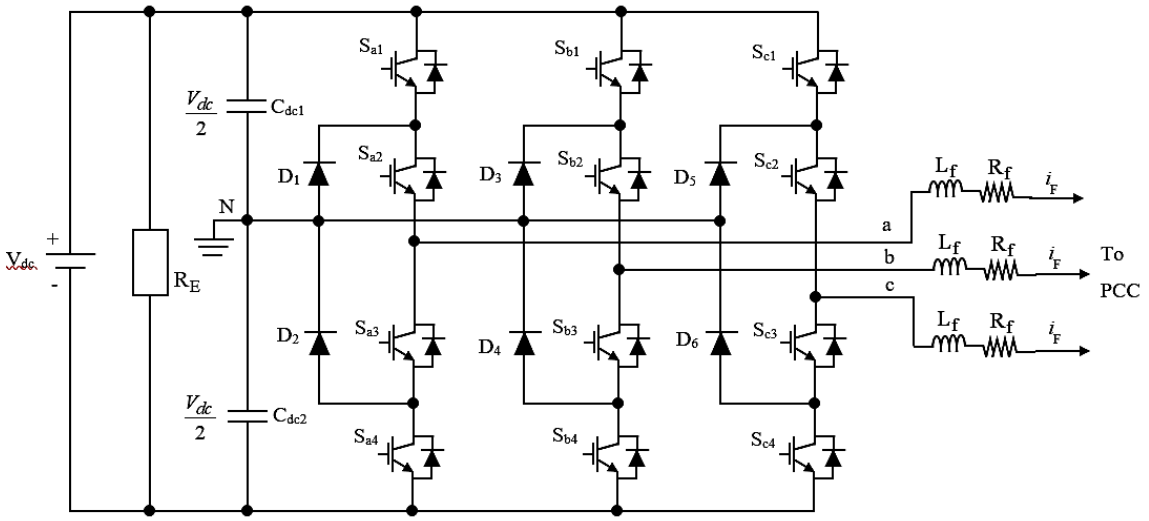

Figure 3.9 The Three Level Neutral Point Clamped Voltage Source Inverter

Table 3.1 Switching States of the Three – Level Neutral Point Clamped VSI

State of Switches				Voltage Level
S_{a1}	S_{a2}	S_{a3}	S_{a4}	
1	1	0	0	$\frac{V_{dc}}{2}$
0	1	1	0	0
0	0	1	1	$\frac{-V_{dc}}{2}$

3.6.5 DC Capacitor and DC-Link Bus Voltage

The DC capacitor is meant to serve as energy storage device and also an input source to the inverter. It is located at the DC side of the inverter and also carries the input ripple current. This capacitor is being charged by the inverter itself. Selection of the DC bus voltage, $V_{dc\text{-}ref}$ and capacitance of the capacitor value, C_{dc} need special attention as both have influence on the output voltage, V_F generated by the DSTATCOM. In the determination of the DC voltage, the minimum DC voltage of the VSI of the DSTATCOM should be greater than twice that of the peak of the phase voltage of the distribution system (Bhim *et al*., 2015). The determination of the DC voltage and capacitor value was done based on Equations (3.33) and (3.34) (Ahmet *et al*., 2015).

$$V_{dc\text{-}ref} = \frac{\sqrt{2}V_{LL}}{m_i} \tag{3.33}$$

$$C_{dc} = \frac{3S_n nT}{(1.8V_m)^2 - (1.4V_m)^2} \tag{3.34}$$

where, C_{dc} = DC capacitor in farad

V_{LL} = line–to–line grid voltage in volts

V_m = peak value of the grid phase voltage in volts

S_n = power rating of the system in kVA

T = time period of the system in seconds

n = cycle that starts to operate the controller

From Figure 3.1 the DC current, I_{dc} is the current through the capacitor, C_{dc}. This current charges or discharges the capacitor.

Equalising resistance

When capacitors are placed in series, it is difficult to have the same voltage across each capacitor. This may be due to the differences in the dielectric insulation resistance of the individual capacitors. In this work, equalising resistor, R_E is used to overcome the problem of voltage variation across the two DC capacitors being used as a storage device. The value of the equalising (balancing) resistor is calculated using the expression given in Equation (3.35) (Anon., 2013a).

$$R_E = \frac{10}{C} \tag{3.35}$$

where, R_E = equalising resistance in ohms

C = capacitance in microfarads

3.6.6 Inverter Output Filter

The interface inductor, L_f serves as a filter inductor used to filter out the high-frequency components in order to shape the compensating current injected at PCC. The inductor filter is said to be the first order filter suitable for high switching frequency inverters. The value of the interfacing inductance is selected based on the compensating current, i_F. It can be calculated for by applying the expression as given in Equation (3.36) (Bhim *et al*., 2015).

$$L_f = \frac{\sqrt{3} m_i V_{dc}}{12 a f_s I_{crp}} \tag{3.36}$$

where, L_f = interface inductor in henry

a = overloading factor

I_{crp} = current ripple in amperes

f_s = switching frequency in hertz

3.6.7 Sinusoidal Pulse Width Modulation Voltage Controller

Sinusoidal Pulse Width Modulation (SPWM) is a type of carrier-based pulse width modulation. In the SPWM technique, a sinusoidal waveform is normally produced by filtering a varying width output of the pulse waveform. The quality of the sine wave depends on the switching frequency of the SPWM (Ahuja and Kumar, 2014). The switching frequency is referred to as carrier frequency whiles that of the fundamental sine wave is called modulation frequency. The switching frequency is chosen to be much higher than the fundamental frequency of the voltage signal. According to Wang *et al*. (2015) the ratio of the switching frequency and fundamental frequency of the voltage signal should be a multiple of 3 for a better reduction of THD.

The principle of operation of SPWM is based on comparing the carrier signal and the pure sinusoidal modulation signal. The PWM control requires generation of both reference and carrier signals that feed into a comparator which then creates modulated pulses depending on the difference between the signals as shown in Figure 3.10 and Figure 3.11 (Ali, 2014). The opening and closing times of the switches are determined by the point of intersection between the reference waveform and the carrier waveform. In this research, a three phase SPWM is used as the gate signal generator for the three level NPC VSI. A carrier voltage waveform is therefore compared with three sinusoidal control voltages which are 120^{o} out of phase with each other. The relative levels of the waveforms are used to control the switching of the device in each phase leg of the inverter. Equation (3.37) gives the frequency modulation ratio of the system.

$$m_r = \frac{f_c}{f_m} \tag{3.37}$$

where, m_r = modulation ratio

f_c = carrier frequency in hertz

f_m = fundamental frequency in hertz

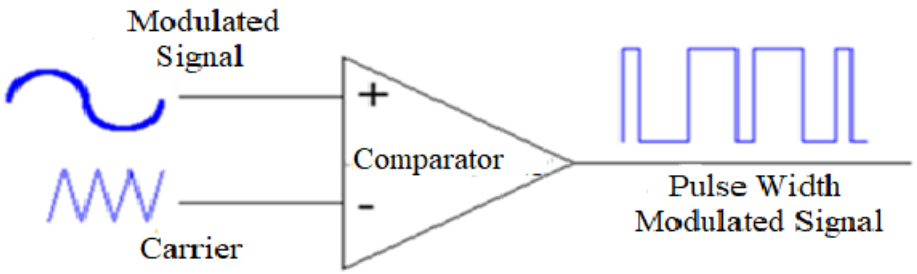

Figure 3.10 Simplified Model of a Comparator

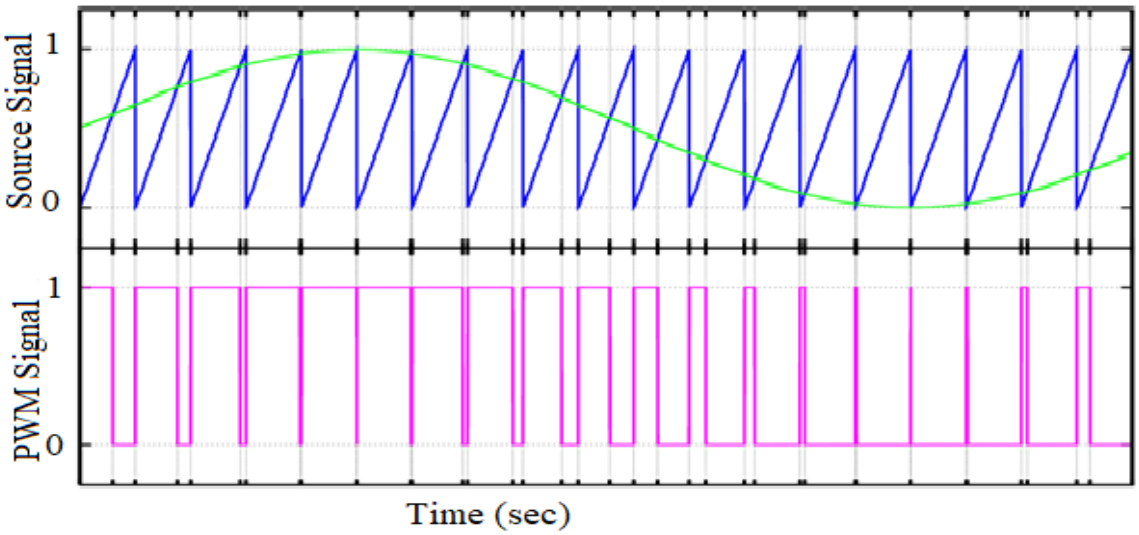

Figure 3.11 An Illustration of Pulse Width Modulation

3.6.8 Control System

The control system regulates the voltage and current. It comprises two loops: the major voltage loop and the minor nonlinear load current loop in cascade. The voltage loop is to keep the voltage, V_{dc} constant in order to safeguard harmonic current generated by nonlinear load. The current loop is to generate the appropriate current, i_F that is to be injected into the PCC via the filter at the output of the inverter, in order to mitigate the harmonic current generated by the nonlinear load. Effectiveness of the control system requires a good design that assures of the needed robustness.

3.7 Design of the Control System

The control system design includes two sets of controllers: A dc voltage controller providing reference signal to the control system in order to maintain the voltage, V_{dc} constant and the current controllers which generate switching signals based on the reference and the measured signals. Figure 3.12 shows the block diagram of the control structure of the DSTATCOM, whilst Figure 3.13 illustrates the general block diagram of the closed loop control system. The simplified version of the control system is presented in Figure 3.14 and Figure 3.15 depicts the voltage and current control loops.

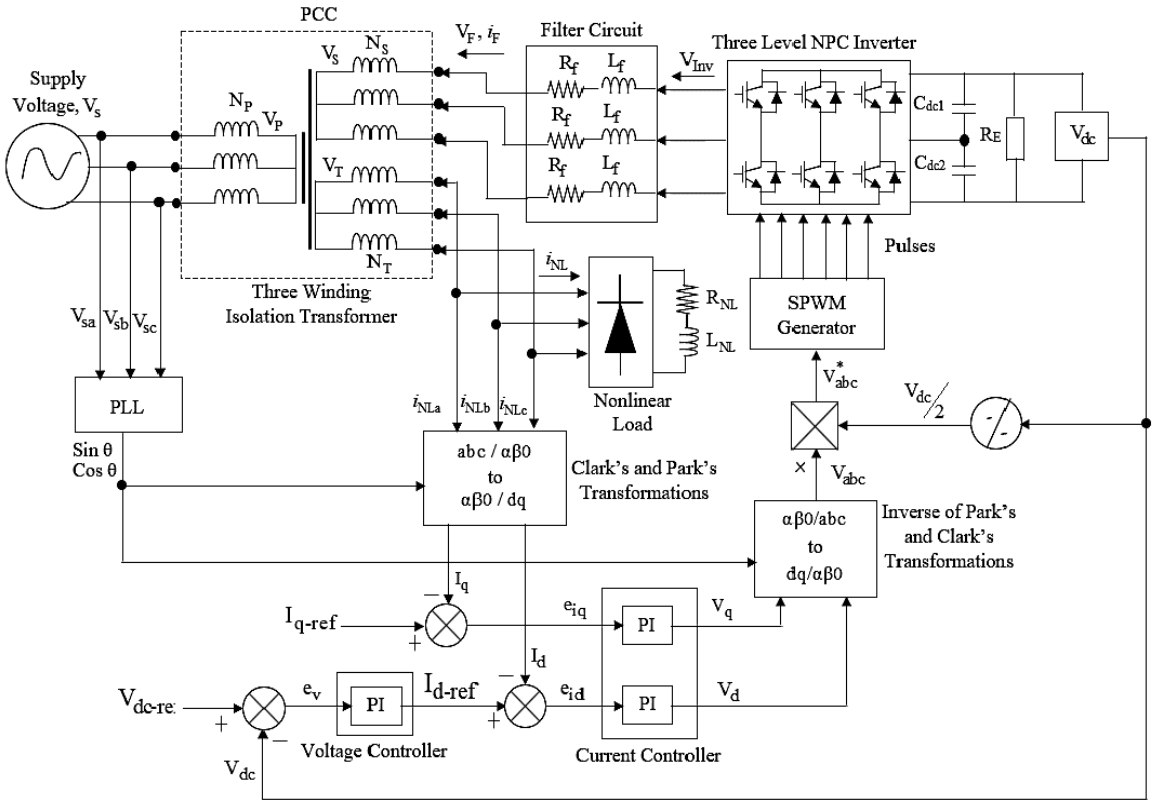

Figure 3.12 Block Diagram of the Control Structure of DSTATCOM

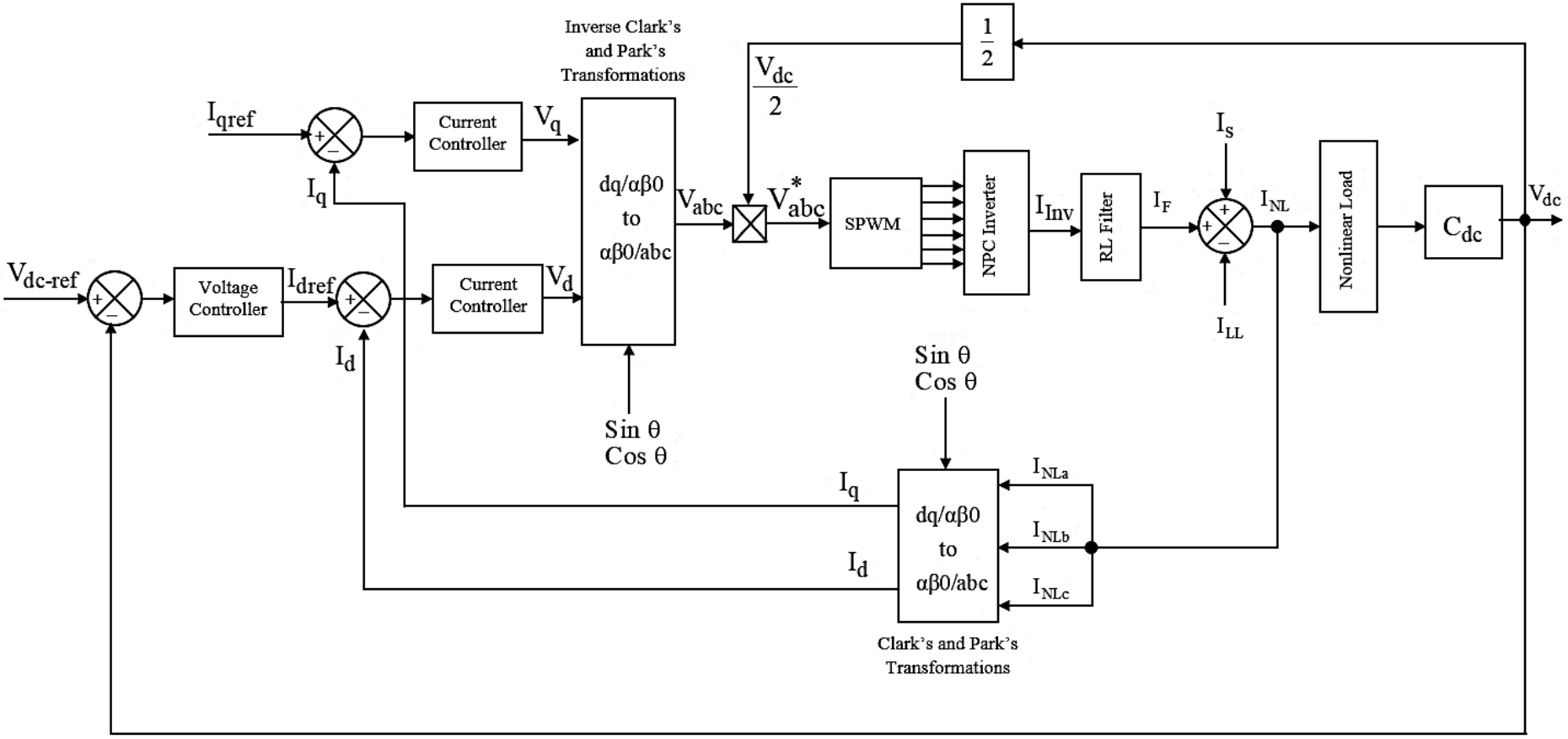

Figure 3.13 General Block Diagram of the Closed Loop Control System

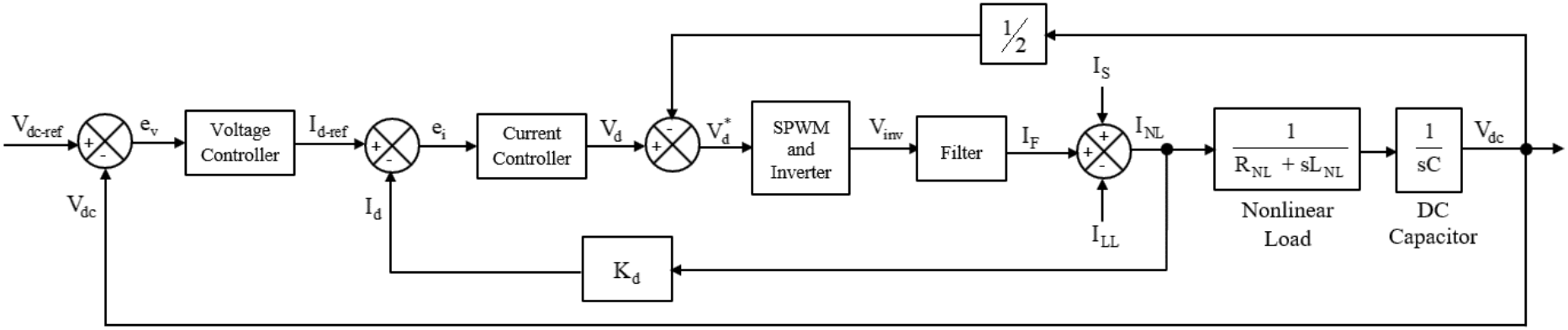

Figure 3.14 Simplified Block Diagram of the Control System

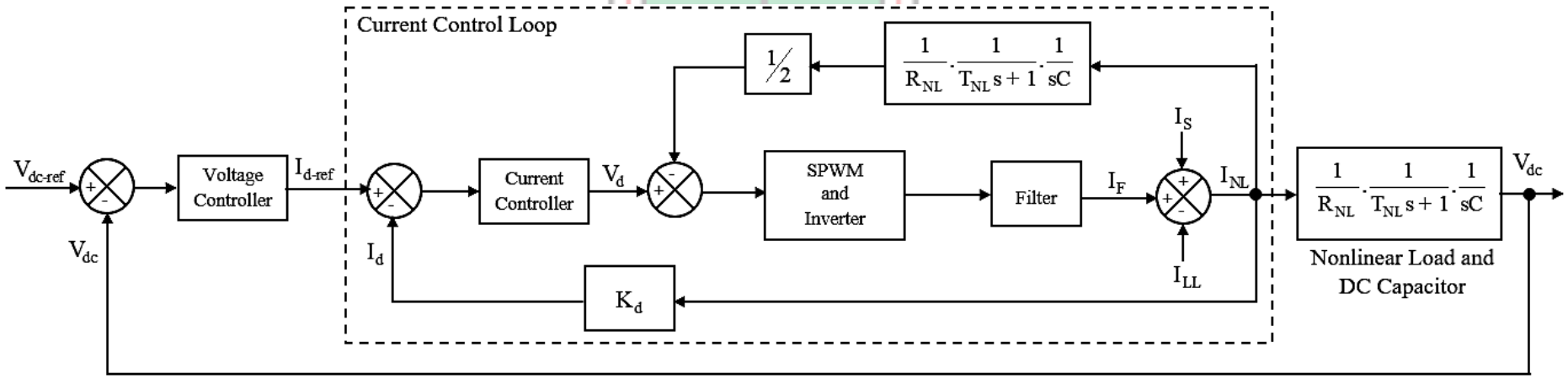

Figure 3.15 Block Diagram depicting the Voltage and Current Control Loops

3.7.1 Governing Equations of the Control System

The closed loop control system can be found in Figure 3.13. The d-q frame was used in the implementation of the current control loop in this model. There are two separate PI current controllers inside the current loop which represent the direct (d) and quadrature (q) currents that produce V_d and V_q reference voltages, respectively.

For the sake of simplicity, and with the fact that the d and q axis will have similar form of equations, only the d-axis equations will be used for analysis hence the q-axis elements are not included in Figure 3.14. With reference to Figure 3.14, the current controller transforms the error obtained after comparison of the reference current, $I_{d\text{-}ref}$ with the measured, I_d component of current into the voltage value V_d. The representative transfer function of the PI current controller is as given by Equation (3.38). The governing equations for the error and the d-axis PI current controller are given by Equations (3.39) and (3.40), respectively.

$$\frac{V_d(s)}{e_i(s)} = K_{pc} + \frac{K_{ic}}{s} \tag{3.38}$$

$$e_i(s) = I_{dref}(s) - I_d(s) \tag{3.39}$$

$$V_d(s) = e_i(s)\left(K_p + \frac{K_i}{s}\right) = \left(I_{dref}(s) - I_d(s)\right)\left(K_{pc} + \frac{K_{ic}}{s}\right) \tag{3.40}$$

where, $V_d(s)$ = Laplace transform of output signal of current controller

$e_i(s)$ = Laplace transform of error signal at the input of current controller

$I_d(s)$ = Laplace transform of the direct axis current signal in amperes

$I_{dref}(s)$ = Laplace transform of the reference direct axis current signal in amperes

K_{pc} = proportional gain of current controller

K_{ic} = integral gain of current controller

The voltage controller as can be found in Figure 3.14 is a DC-link capacitor voltage controller. The output voltage, V_F of the DSTATCOM is generated by the VSI operated from the DC-link capacitor. Therefore, the main function of the PI voltage controller is to

control the DC capacitor voltage, V_{dc} in order to maintain a constant voltage across the storage capacitor, C_{dc}. To maintain a constant DC-link voltage, it is required to calculate the error, e_v by subtracting the DC capacitor voltage, V_{dc} from the reference DC voltage, $V_{dc\text{-}ref}$ as given by Equation (3.41). The voltage controller implemented as a PI controller also provides a current setpoint value to the current controller. The representative transfer function of the PI voltage regulator and the output signal of the voltage controller are given in Equations (3.42) and (3.43), respectively.

$$e_v(s) = V_{dc\text{-}ref}(s) - V_{dc}(s) \tag{3.41}$$

$$\frac{I_{d\text{-}ref}(s)}{e_v(s)} = K_{pv} + \frac{K_{iv}}{s} \tag{3.42}$$

$$I_{d\text{-}ref}(s) = e_v(s)\left(K_{pv} + \frac{K_{iv}}{s}\right) = \left(V_{dc\text{-}ref}(s) - V_{dc}(s)\right)\left(K_{pv} + \frac{K_{iv}}{s}\right) \tag{3.43}$$

where, $e_v(s)$ = Laplace transform of the error voltage signal

$V_{dc\text{-}ref}(s)$ = Laplace transform of the reference DC voltage in volts

$V_{dc}(s)$ = Laplace transform of the measured DC voltage signal across the storage capacitor C_{dc} in volts

K_{pv} = proportional gain of voltage controller

K_{iv} = integral gain of voltage controller

The signal at the output of the inverter voltage is as given in Equation (3.44).

$$V_{inv}(s) = V_d^*(s)\left(\frac{1}{T_{inv}s + 1}\right) \tag{3.44}$$

where, $V_{inv}(s)$ = Laplace transforms of the inverter output voltage signal in volts

$V_d^*(s)$ = Laplace transform of the switching voltage signal at the input of the SPWM in volt

T_{inv} = switching time delay in seconds

Equation (3.45) gives the switching time delay in terms of the switching frequency.

$$T_{inv} = \frac{T_{sw}}{2} = \frac{1}{2f_{sw}} \tag{3.45}$$

where, T_{sw} = switching time constant of the VSI in seconds

f_{sw} = switching frequency in Hz

The transfer function of the filter, nonlinear load and dc capacitor are given by Equations (3.46), (3.47) and (3.48), respectively.

$$G_f(s) = \frac{1}{R_f + sL_f} \tag{3.46}$$

$$G_{NL}(s) = \frac{1}{R_{NL} + sL_{NL}} \tag{3.47}$$

$$G_C(s) = \frac{1}{sC} \tag{3.48}$$

where, R_f = filter resistance in ohms

L_f = filter inductance in henry

R_{NL} = nonlinear load resistance in ohms

L_{NL} = nonlinear load inductance in henry

With regard to Figure 3.14, the following expressions as given in Equations (3.49), (3.50) and (3.51), respectively are deduced for the computations.

$$I_F(s) = V_{inv}(s)\left(\frac{1}{R_f + sL_f}\right) \tag{3.49}$$

$$V_{dc}(s) = I_{NL}(s)\left(\frac{1}{R_{NL} + sL_{NL}}\right)\left(\frac{1}{sC}\right) \tag{3.50}$$

$$I_{NL}(s) = I_F(s) + I_S(s) - I_{LL}(s) \tag{3.51}$$

where, $I_F(s)$ = Laplace transform of the filter output current signal in amperes

$I_{NL}(s)$ = Laplace transform of the nonlinear load current signal in amperes

$I_S(s)$ = Laplace transform of the source current signal in amperes

$I_{LL}(s)$ = Laplace transform of the linear load current signal in amperes

Figure 3.16 establishes the transfer function version of Figure 3.15 whilst that of Figure 3.17 illustrates the implementation of the Figure 3.16 in MATLAB/Simulink software environment. This is done in order to tune the PI controllers and validate the performance of the control system.

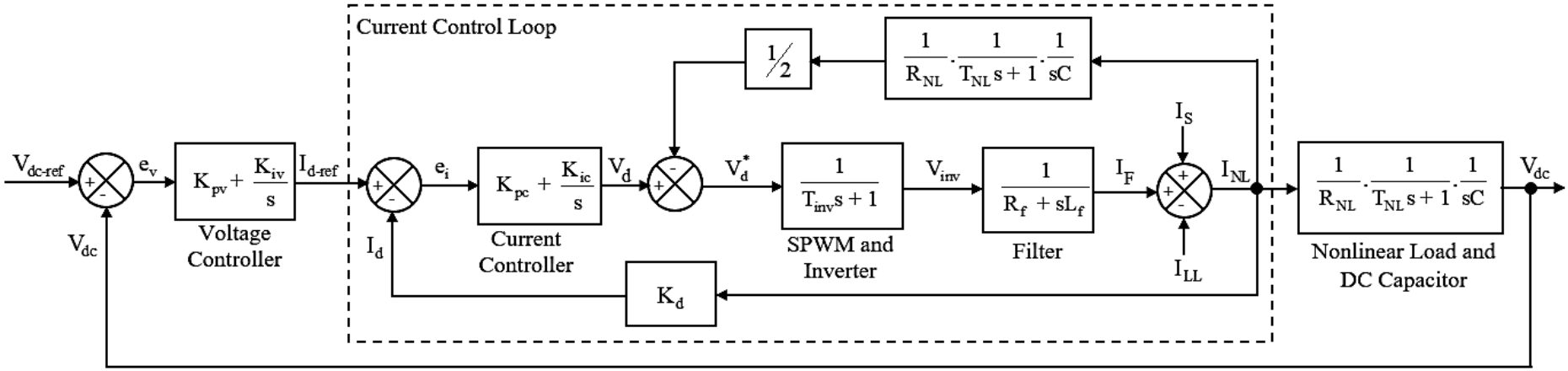

Figure 3.16 Transfer Function Version of the Voltage and Current Control Loops

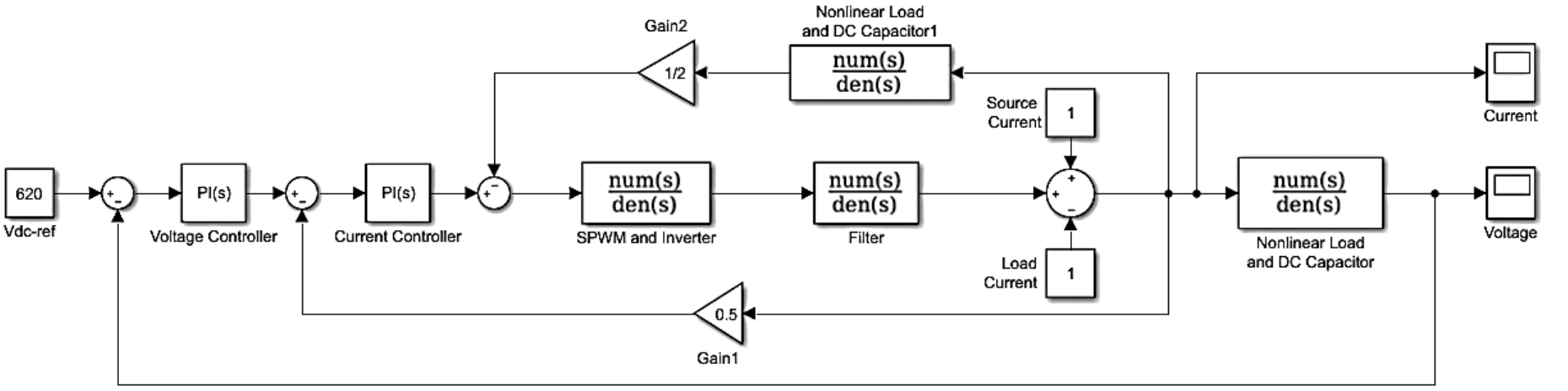

Figure 3.17 Simulink Implementation of the Control System

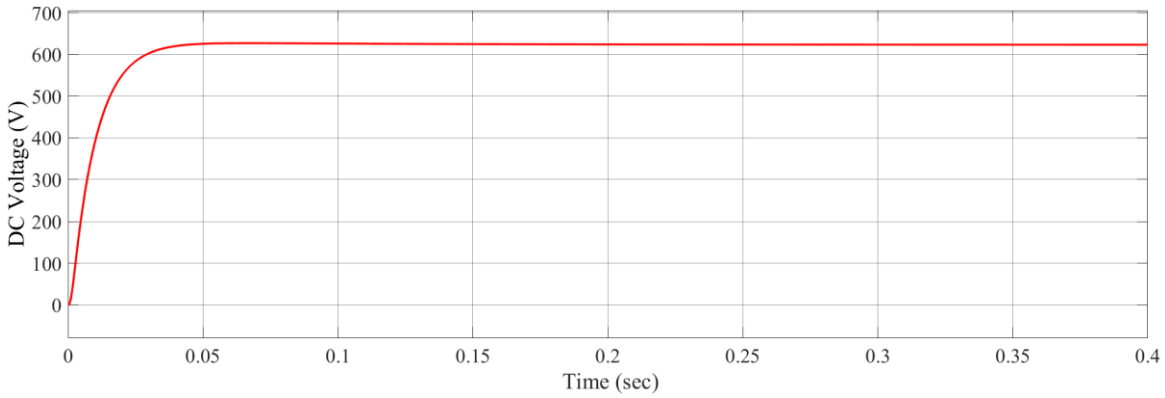

Figure 3.18 Response of the Control System for the First Case

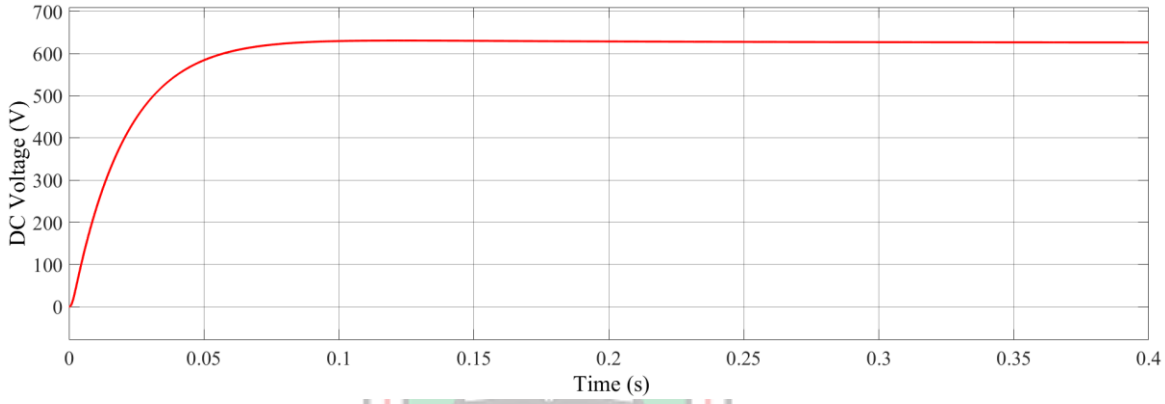

Figure 3.19 Response of the Control System for the Second Case

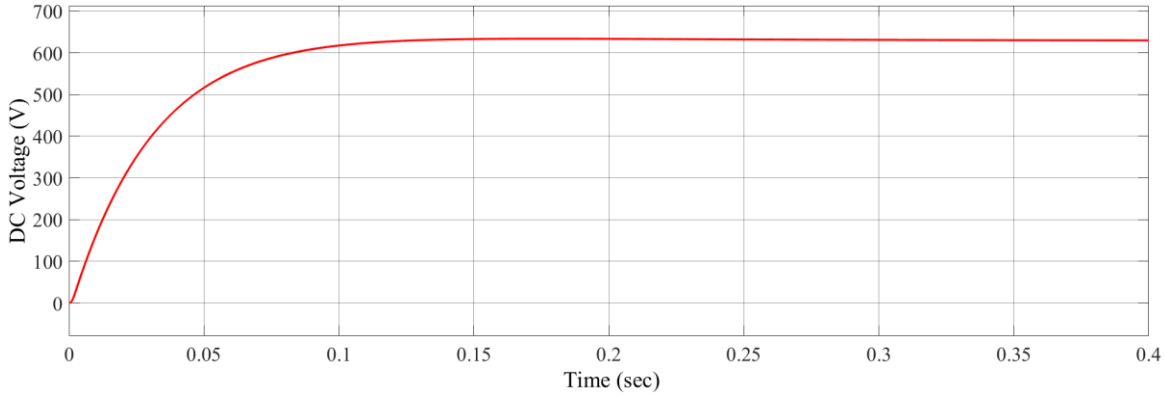

Figure 3.20 Response of the Control System for the Third Case

After the control system design, it was tested by way of simulations for three different cases of nonlinear loading in order to check its robustness. Figure 3.18 shows the response of the control system when the nonlinear load is first of all connected whilst Figure 3.19 illustrates the response of the same control system with a connected nonlinear load which is two times or double the magnitude of the first load. The response in the case of three times or triple of

the first nonlinear loading with its magnitude is also shown in Figure 3.20. Considering the loads connected with their corresponding waveforms, it is observed that with a large magnitude of load current, the rise and settling times of the controller are much greater as compared with the smaller magnitude of load current. The control system serves as the heart of harmonic mitigation. The ability of the control system to maintain a constant voltage, V_{dc} at the input of the NPC inverter determines the magnitude of harmonics that can be mitigated. With reference to Figure 3.18, Figure 3.19 and Figure 3.20, respectively it can be concluded that the control system as an integral part of DSTATCOM is working as expected. Although the magnitude of the connected load influences the rise and settling times, it is able to maintain a constant dc voltage.

3.8 Computer Simulations

Computer simulations were carried out to verify the system's ability to mitigate the nonlinear load generated harmonics and also to confirm, or otherwise, the effectiveness of the control system in regulating the dc capacitor voltage, V_{dc}. This is done when both linear and nonlinear loads are connected to the system and simulated one after the other. The control system design was done and simulated in order to check the response of the PI controllers with respect to the connected loads. The effect of harmonics on the waveform can also be seen through simulations. MATLAB tuning is done on the control system in the course of the simulations. The proportional and integral gains of the voltage and current controllers were obtained as a result of the tuning. The tuned PI controller gains obtained from the designed tuning were used in implementing the system arrangement for determining the total harmonics generated and subsequently mitigated. Figure 3.21 shows the complete circuit implementation of the proposed system in MATLAB/Simscape software environment. The block labeled scope 1 display the source voltage and current waveforms whiles that of scope 3 display the capacitor voltage, V_{dc} as a response of the control system. The C-source codes for the control system can be found at Appendix B.

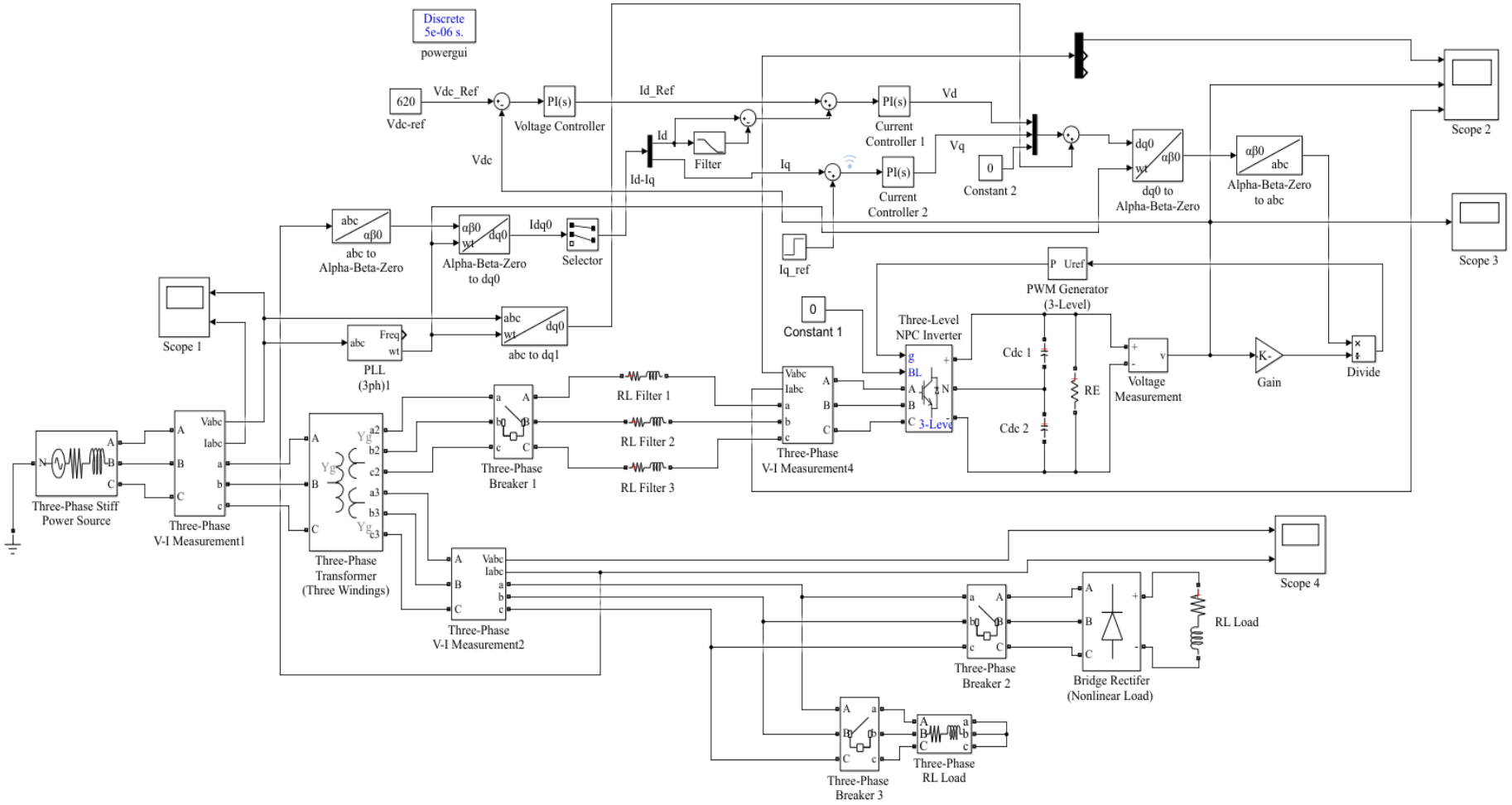

Figure 3.21 The Complete Circuit Implementation of Proposed System in MATLAB/Simulink Software

3.9 Summary

This chapter has presented methods and techniques employed for the accomplishment of this research work. Modelling of the various sections of the proposed system was done. In the circuit design, a stiff power source was used as the supply to the power distribution system where three phase, three winding transformer was used as the PCC. Both linear and nonlinear loads were connected at the PCC. Since the main focus is to mitigate harmonics, three level NPC VSI based DSTATCOM was incorporated to reduce the high harmonics content generated by the nonlinear load. Within the DSTATCOM is the control system together with SPWM, 3-level NPC inverter, output filter, PLL among others. The performance of the DSTATCOM mainly depended on the control system. In conclusion, computer simulations of the system using MATLAB/Simulink software were conducted to confirm the effectiveness of the control system.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Introduction

There are many techniques which can be used to mitigate current harmonics. This chapter presents the simulation results after using DSTATCOM at the PCC on a power distribution system. The power distribution system with the DSTATCOM was simulated in MATLAB/Simulink environment using Simulink blocks. Results presented in this chapter are the simulation results with reference to the stated objectives.

4.2 Simulation Test Results on the System

The system parameters used for the simulations are given in Table 4.1. The supply voltage of the power distribution system is 400 V with the line frequency of 50 Hz.

Table 4.1 System Parameters used in the Simulation

SN	System Parameter	Parameter Value
1.	Source Voltage and Frequency	V_s = 400 V , 50 Hz
2.	Source Impedance	R_s = 0.1 Ω , L_s = 0.01 mH
3.	Linear Load	R = 50 Ω, and L = 0.01 mH
`4.	DC Bus Voltage	V_{dc} = 620 V
5.	DC - link Capacitor	$C_{dc1} = C_{dc2}$ = 100 μF
6.	Equalising Resistance	R_E = 15 kΩ
7.	Filter Inductance and Resistance	L_f = 95 mH R_f = 8 Ω
8.	PI Voltage Controller	K_p = 1.09 K_i = 0.38
9.	PI Current Controller	K_p = 0.16 K_i = 0.000304

The line-to-line output voltage of the three-level NPC VSI which corresponds to the time interval of $0 \leq t \leq 0.4$ s is shown in Figure 4.1. The line-to-line output voltage comprises three levels of square waveform (or staircase) which is close to sinusoidal waveform.

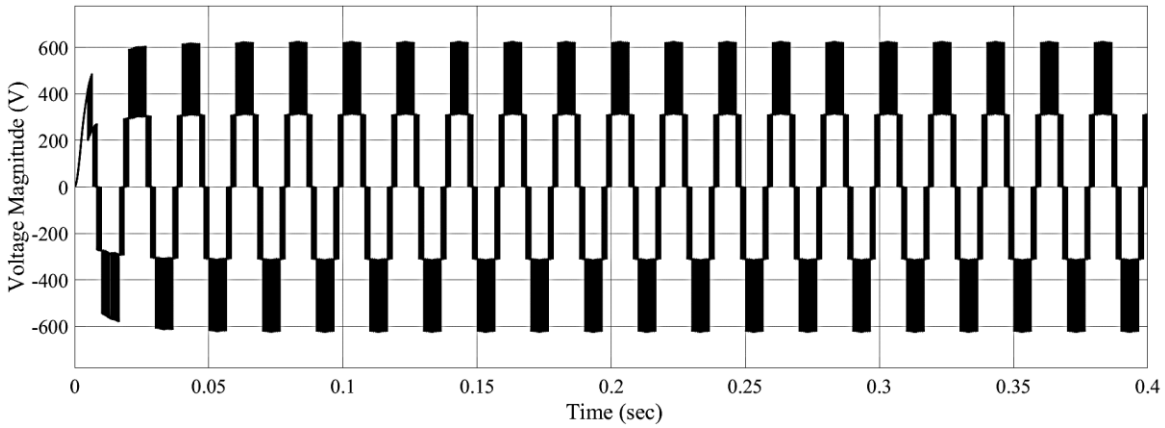

Figure 4.1 Line – to – Line Stepped Output Voltage of 3-Level NPC VSI

The voltage across the energy storage capacitor C_{dc} which has been maintained at a DC voltage of 620 V is shown in Figure 4.2. This shows that the control system is able to maintain the constant voltage, V_{dc}.

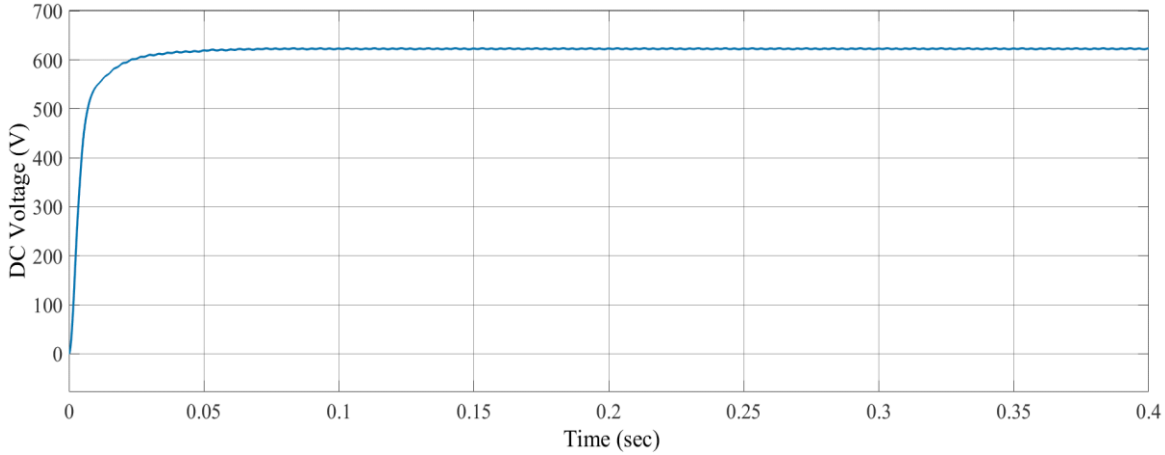

Figure 4.2 Response of the Control System

Figure 4.3 is the source voltage and current waveforms when a linear load was connected. It is to be noted that for a linear load, the harmonic is negligibly small such that it can be neglected. Both voltage and current waveforms therefore appear to be undistorted and normally referred to as pure sinusoidal waveforms.

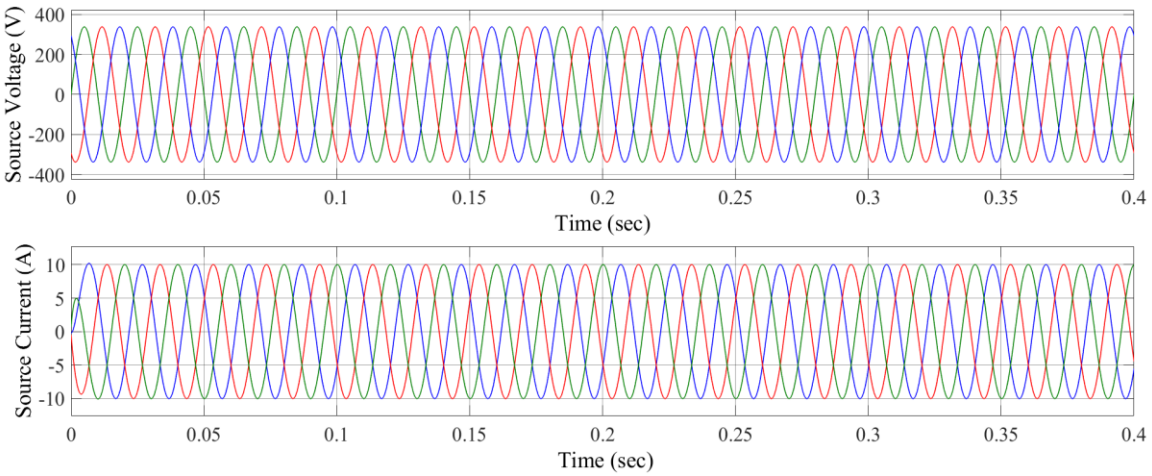

Figure 4.3 Source Voltage and Current Waveforms with Linear Load Connected

4.3 Simulation Results with and without DSTATCOM

Figure 4.4 shows another line-to-line output voltage of the three-level NPC VSI and the corresponding dc capacitor voltage. In this case, a nonlinear load was connected which corresponded to the time interval of $0 \leq t \leq 0.4\,s$ and DSTATCOM was also connected at the PCC through a circuit breaker at the time interval of $0.2\,s \leq t \leq 0.4\,s$. This demonstrates the response of DSTATCOM to sudden changes in the circuit. The corresponding waveforms of the source voltage and current are shown in Figure 4.5. In Figure 4.5, it can be seen that at time interval of $0 \leq t \leq 0.2$ s, the current waveforms are distorted with harmonics and were mitigated between the period of 0.2 s ≤ to ≤ 0.4 s as a result of the DSTATCOM been connected. This validates the responsiveness of DSTATCOM with regard to current harmonics reduction.

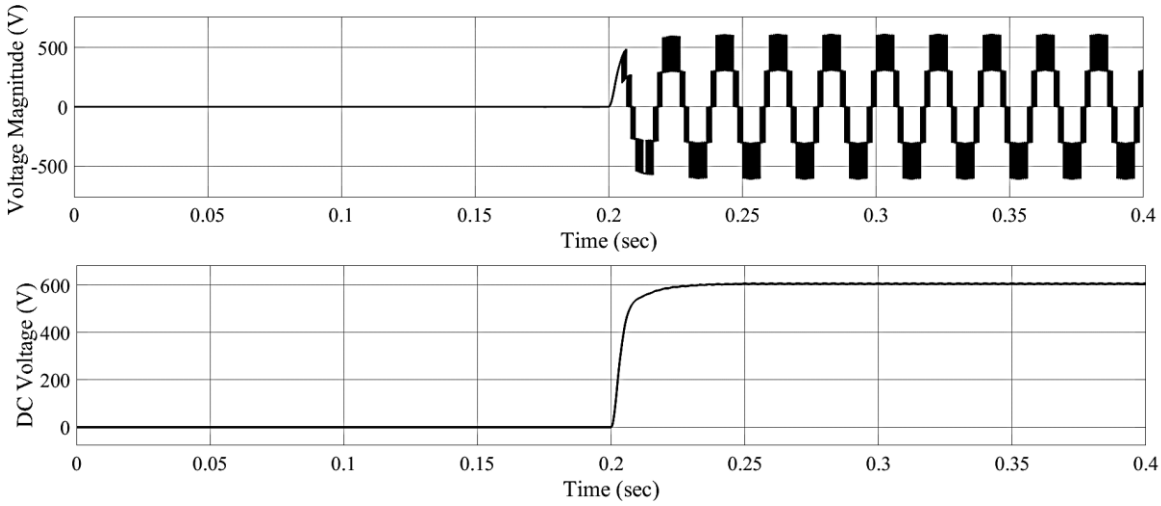

Figure 4.4 Line-to-Line Output Voltage of VSI and Response of the System

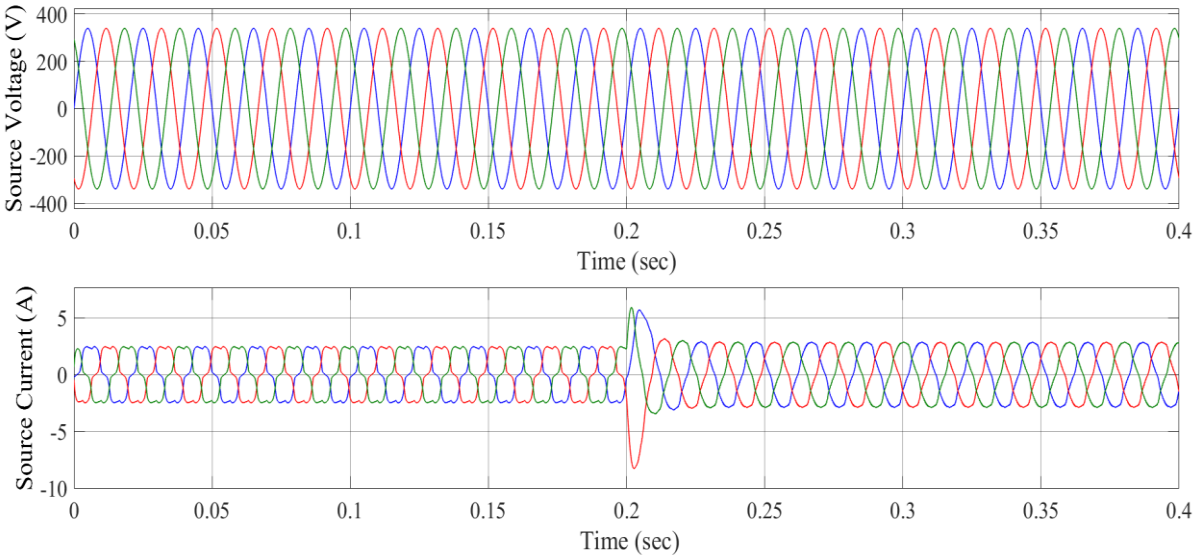

Figure 4.5 Source Voltage and Current Waveforms for Nonlinear Load with DSTATCOM Connected at 0.2 secs

As a way of checking the consistency in the performance of the control system in the DSTATCOM, three different nonlinear loads were connected to the power distribution system one after the other. These nonlinear loads are classified as Load 1, Load 2 and Load 3 with the values $R_{NL} = 100\ \Omega,\ L_{NL} = 0.01\ mH$; $R_{NL} = 200\ \Omega,\ L_{NL} = 0.02\ mH$; and $R_{NL} = 300\ \Omega,\ L_{NL} = 0.03\ mH$, respectively. Figure 4.6 shows the source voltage and current waveforms after connecting load 1 to the system. It can be seen that there have been harmonics generated by the nonlinear load. Whilst the voltage waveforms remained purely sinusoidal, the current waveforms became distorted. This effect of current distortion is in this research referred to as the current harmonics.

Fast Fourier Transform (FFT) analysis is one of the most important tools normally used in finding the percentage of the THD caused in an ideal waveform due to the disturbances as a result of nonlinear load. In this research, FFT analysis of the source current was performed using “powergui”. The powergui is the block which gives a series of possibilities for tuning and understanding its operation. The result of FFT analysis carried out on source current waveforms of Figure 4.6 is shown in Figure 4.7. It has been observed from the result of FFT analysis that; the percentage of harmonic content generated due to the nonlinear load on the system is 12.92%. On the other hand, Figure 4.8 shows the results of the FFT analysis on the current waveform after the application of the DSTATCOM on the system. The THD

reduced to 5.71%. In this case, the investigation with DSTATCOM for installation on power distribution system for harmonics reduction has been demonstrated successfully.

Figure 4.6, Figure 4.7 and Figure 4.8, show the results for “Load 1”. Figure 4.9 illustrates the corresponding response of the control system. Load 1 serves as the base case for the other two loads. The “Load 2” connected to the system is double that of “Load 1” whilst that of “Load 3” is three times or triple that of “Load 1”. These three categories of load are nonlinear. The FFT analysis is also carried out on the other two loads to check the THD before and after connecting the DSTATCOM. Their results are shown in Figure 4.10, Figure 4.11, Figure 4.12 and Figure 4.13 for “Load 2” whilst that of “Load 3” are shown in Figure 4.14, Figure 4.15, Figure 4.16 and Figure 4.17. Figure 4.13 and Figure 4.17 illustrated the response of the control system with respect to the “Load 2” and “Load 3”.

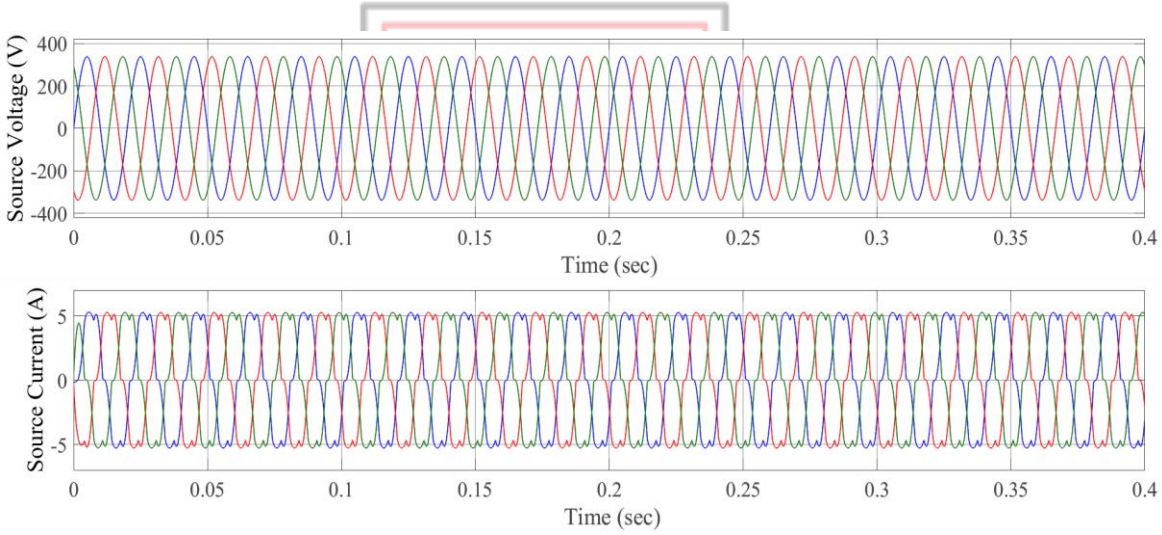

Figure 4.6 Source Voltage and Current Waveforms with Nonlinear Load 1 without DSTATCOM

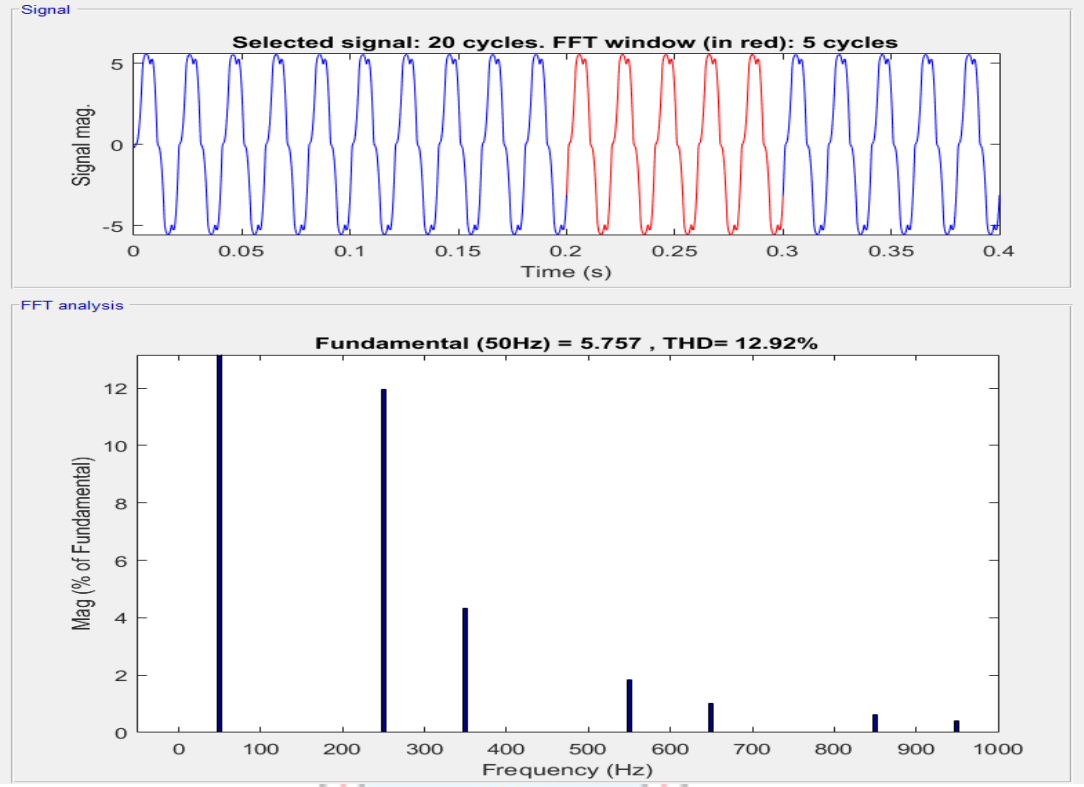

Figure 4.7 Result of FFT Analysis of Source Current without DSTATCOM showing Waveform and Spectrum

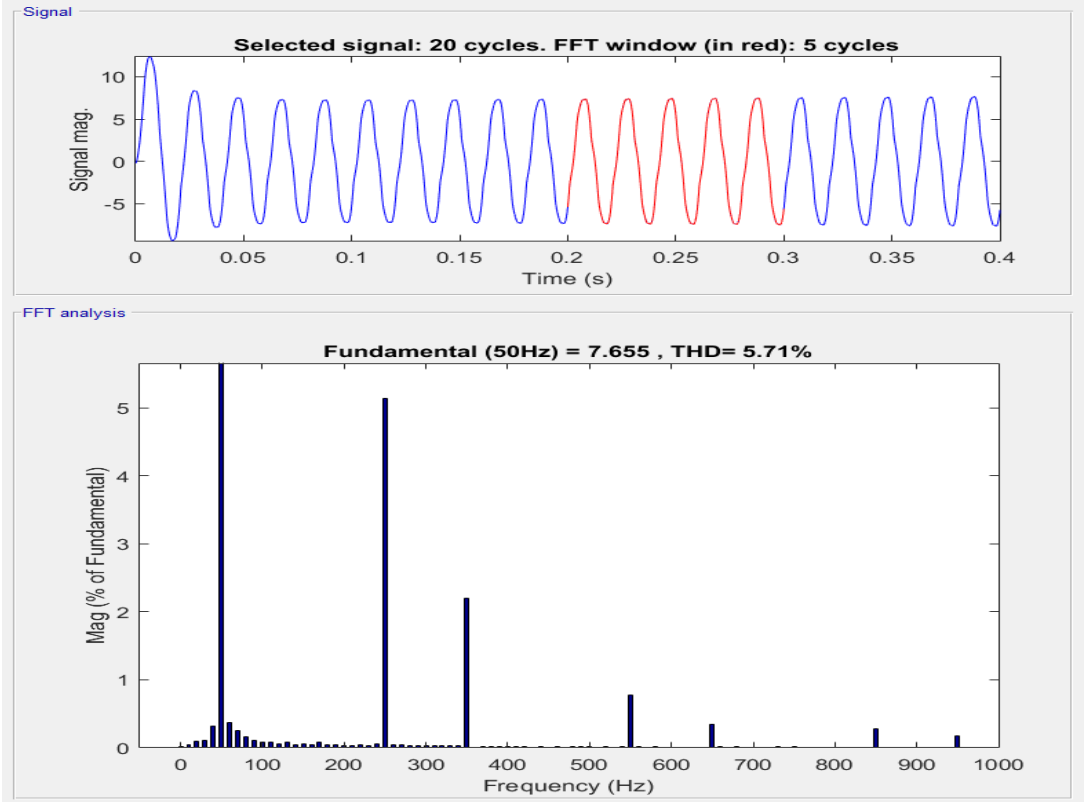

Figure 4.8 Result of FFT Analysis of Source Current with DSTATCOM showing Waveform and Spectrum

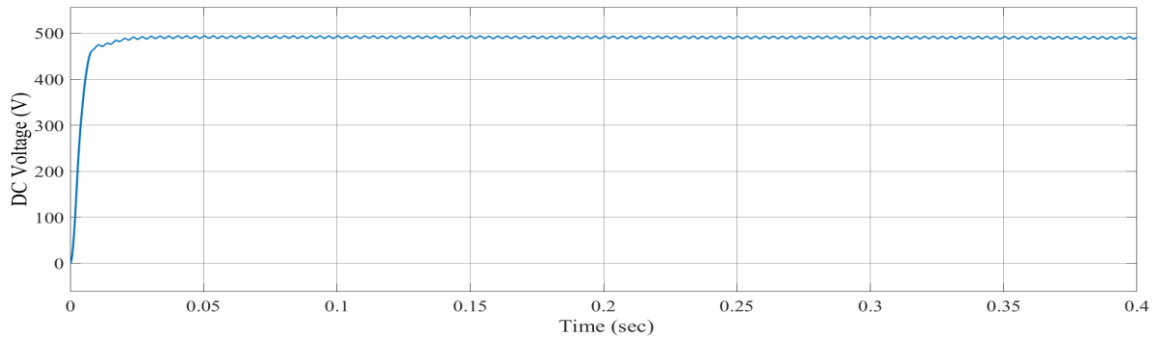

Figure 4.9 Response of the Control System when "Load 1" is Connected

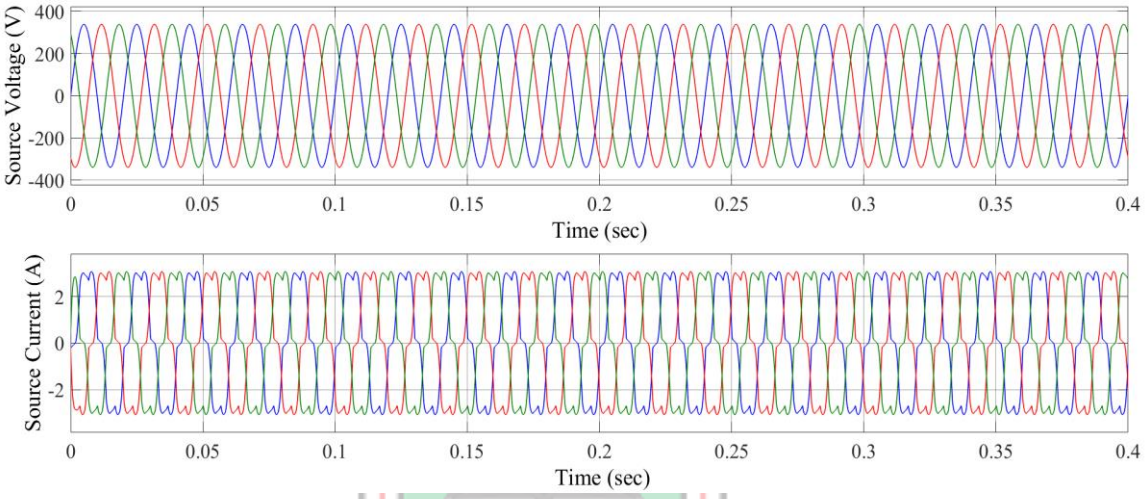

Figure 4.10 Source Voltage and Current Waveforms with Nonlinear Load 2 without DSTATCOM

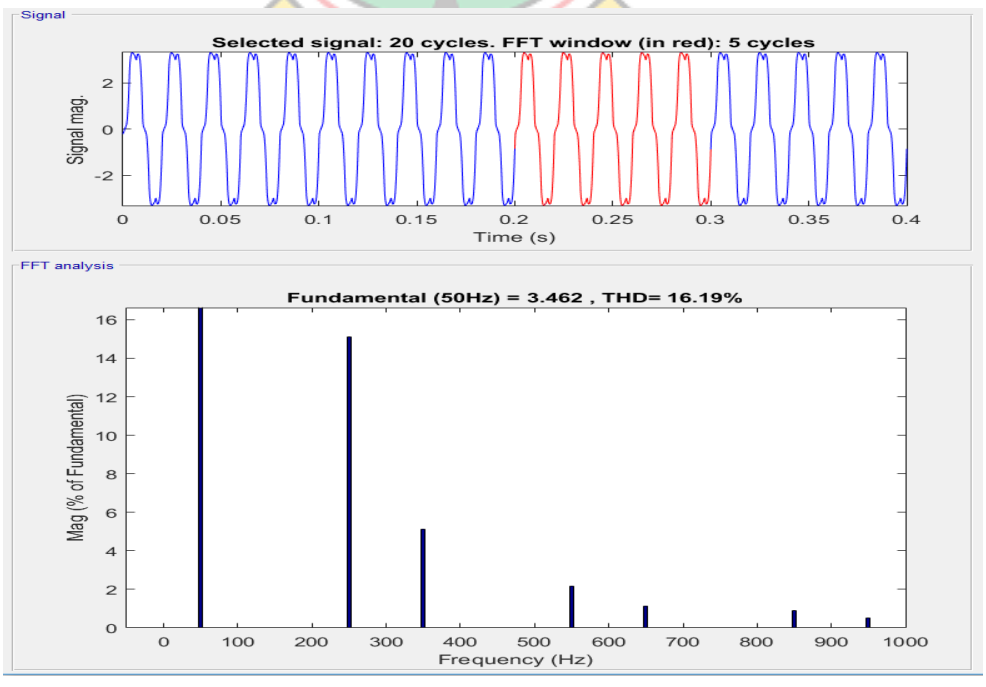

Figure 4.11 Result of FFT Analysis of Source Current without DSTATCOM showing Waveform and Spectrum

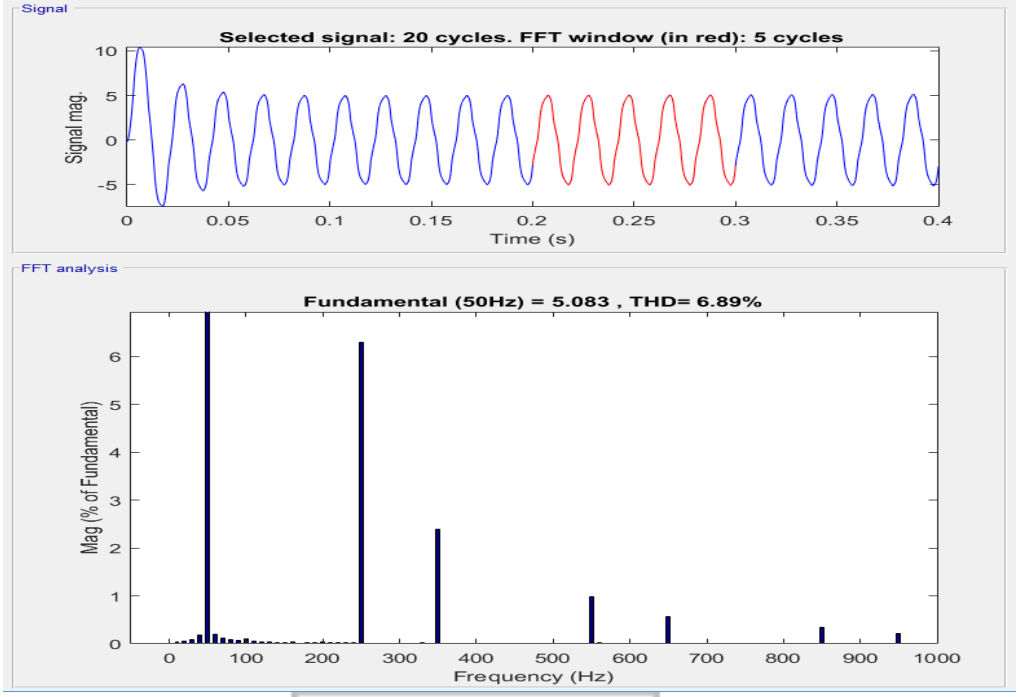

Figure 4.12 Result of FFT Analysis of Source Current with DSTATCOM showing Waveform and Spectrum

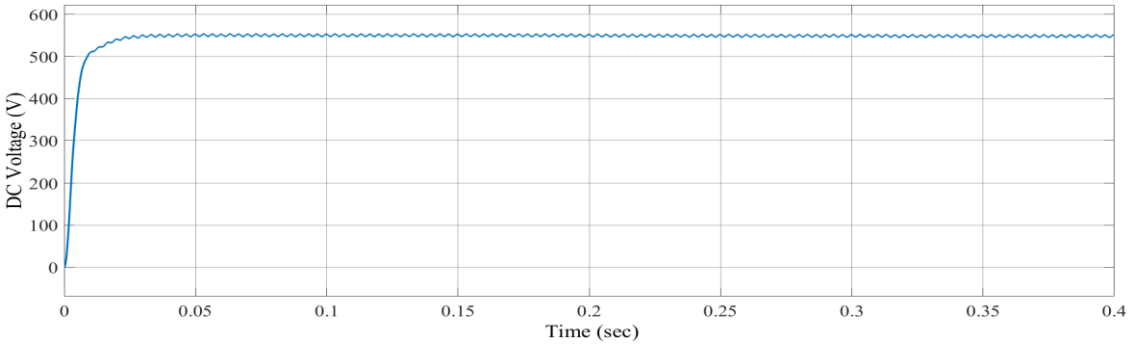

Figure 4.13 Response of the Control System when "Load 2" is Connected

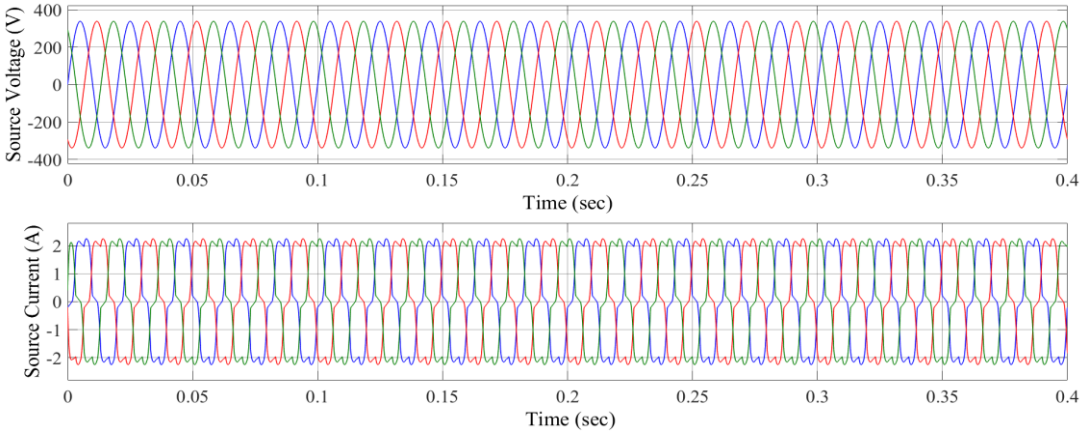

Figure 4.14 Source Voltage and Current Waveforms with Nonlinear Load 3 without DSTATCOM

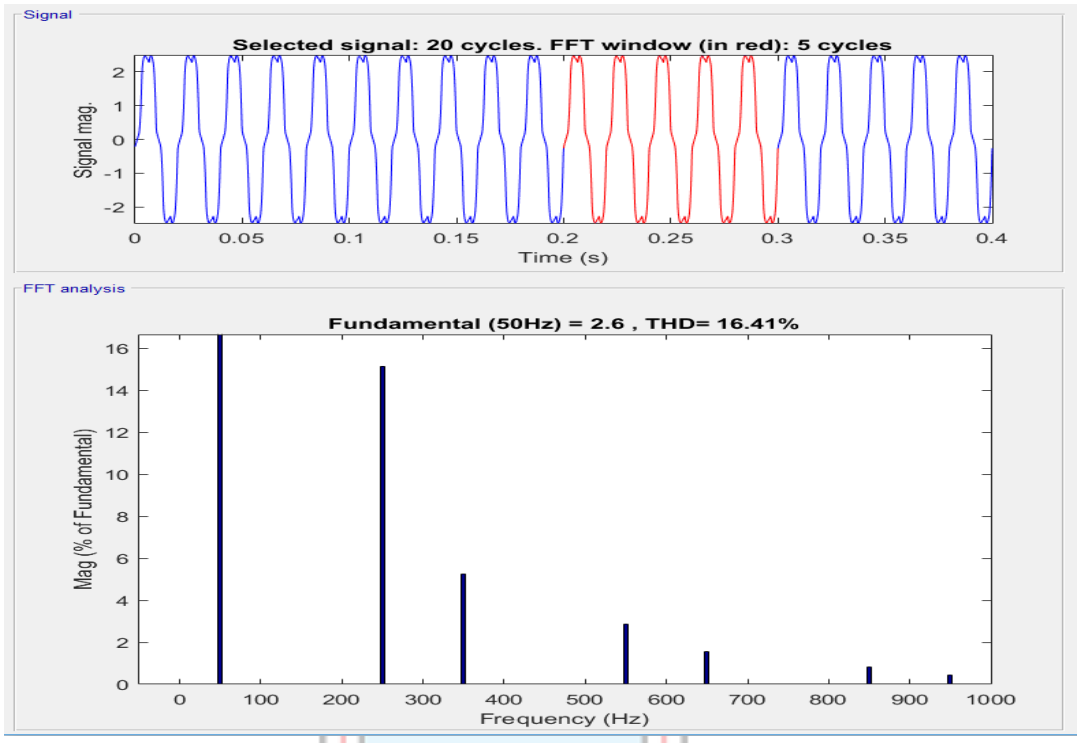

Figure 4.15 Result of FFT Analysis of Source Current without DSTATCOM showing Waveform and Spectrum

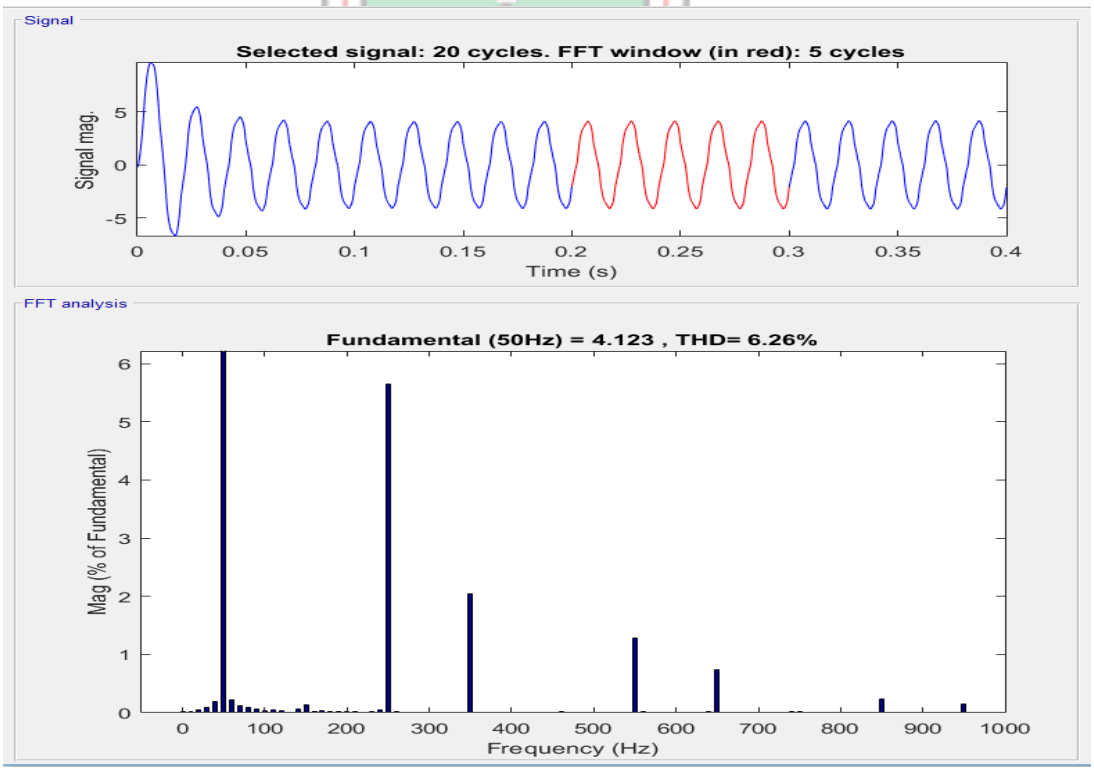

Figure 4.16 Result of FFT Analysis of Source Current with DSTATCOM showing Waveform and Spectrum

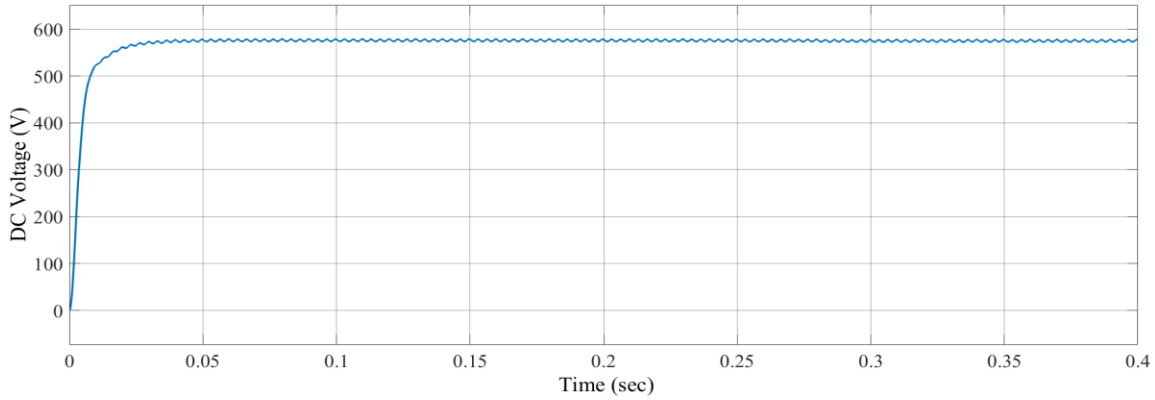

Figure 4.17 Response of the Control System when "Load 3" is Connected

From the control system response graph, it can be noticed that the magnitude of the load affects the response of the control system and hence influences the level of percentage reduction of the harmonic content in the system. Table 4.2 shows the three categories of the nonlinear load, and the corresponding magnitudes of THD and their levels of mitigation accomplished by DSTATCOM.

Table 4.2 Total Harmonic Distortion of the Source Current, i_S before and after Mitigation

SN	Nonlinear Load	Before Mitigation %THD_I	After Mitigation %THD_I
1.	Load 1: R_{NL} = 100 Ω, L_{NL} = 0.01 mH	12.92	5.71
2.	Load 2: R_{NL} = 200 Ω, L_{NL} = 0.02 mH	16.19	6.89
3.	Load 3: R_{NL} = 300 Ω, L_{NL} = 0.03 mH	16.41	6.26

From Table 4.2 the percentage harmonic reduction is calculated as follows:

$$\text{Percentage reduction} = \frac{\text{Initial value} - \text{Final value}}{\text{Initial value}} \times 100\%$$

$$= \frac{12.92 - 5.71}{12.92} \times 100\%$$

$$= 55.8\%$$

This calculation is based on load 1 due to the fact that its mitigation level which stood at 5.71 is closer to the permissible standard as indicated in Appendix A.

4.4 Summary of Findings

The summary of findings of this research are presented as follows:

i. Total current harmonic levels of 12.92%, 16.19% and 16.41% got reduced to 5.71%, 6.89% and 6.26%, respectively by virtue of the responsiveness of SRF theory-based DSTATCOM;

ii. At a nonlinear loading level of $R_{NL} = 100\ \Omega$, $L_{NL} = 0.01\text{mH}$, the mitigated harmonics stood at 5.71% which is still higher than the harmonics standard value of 5% and below (see Table A1 of Appendix A);

iii. Control system performance for the nonlinear loading of $R_{NL} = 100\ \Omega$ $L_{NL} = 0.01\ \text{mH}$; $R_{NL} = 200\ \Omega$, $L_{NL} = 0.02\ \text{mH}$; $R_{NL} = 300\ \Omega$, $L_{NL} = 0.03\ \text{mH}$ gave steady state voltage values of 489 V, 555 V and 575 V, respectively as against a reference voltage of 620 V. The corresponding settling times were 0.025 secs, 0.022 secs, and 0.21 sec respectively; and

iv. From Figure 4.7 the nonlinear load generated fifth and seventh harmonics with the percentage magnitude of 12% and 4%, respectively with third harmonics being zero; DSTATCOM reduced the nonlinear load harmonic generated by 55.8%.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

Power quality problem is as a result of the increasing rate of use of power electronics equipment's normally referred to as nonlinear loads. In order to maintain the quality of power, the problems affecting the power quality must be treated efficiently. Among the different types of power quality problems, harmonics is one of the dangerous factors that lead to power quality problem in power distribution systems. The design of the system which comprises the power distribution system, the DSTATCOM and the connected load was done successfully. Modelling and implementation of the system using MATLAB/Simulink software was also done successfully. Constituting the DSTATCOM is the DC voltage, VSI and the control system. Among these three things the control system plays a crucial role in the performance of the DSTATCOM. From this research the following conclusion were drawn:

i. DSTATCOM is able to mitigate some desirable percentage of harmonics at PCC thereby preventing the harmonics generated by consumers' nonlinear load from reaching the supply source where it will generate into voltage harmonics;
ii. The percentage magnitude of THD_I reduction depends solely on the responsiveness of the designed control system of DSTATCOM; and
iii. DSTATCOM performance is highly dependent on the reference tracking effectiveness of the control system. Further desirable performance of the control system will require improvements in tuning the voltage and current controllers.

5.2 Recommendations

The following are the recommendations based on the findings and conclusions drawn from the research conducted:

i. DSTATCOM is recommended for use in reducing current harmonics levels generated by nonlinear loads in distribution systems. However, its control system requires further improvement; and

ii. Artificial intelligence techniques need to be employed in tuning and optimizing the voltage and current controllers of the DSTATCOM.

5.3 Research Contributions

The research contributions are registered as follows:

i. Use of SRF theory-based DSTATCOM in mitigating current harmonics content generated by nonlinear loads in power distribution systems; and
ii. Successful design of the control system of DSTATCOM and use of three winding isolation transformer for the purpose of current harmonics mitigation in low voltage distribution systems.

5.4 Future Research Directions

Continuation of this research entails the following:

i. Further research should explore use of multi-source multilevel inverters such as the H-bridge in place of the three level NPC VSI of the DSTATCOM; and
ii. Optimisation algorithms such as Particle Swarm Optimisation (PSO), Bacteria Foraging Optimisation Algorithm (BFOA), and Gravitational Search Algorithm (GSA) should be employed in tuning the controllers of the control system of DSTATCOM for better performance.

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APPENDICES

APPENDIX A

HARMONICS STANDARDS

Table A1 IEEE 519 Current Distortion Limits

Harmonic Current Limits for Nonlinear Load at the Point of Common Coupling with other Loads, for Voltages ranging from 120 V to 69 kV.						
Maximum Odd Harmonic Current Distortion in % of Fundamental Harmonic Order						
I_{SC}/I_L	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h < 50$	TDD
< 20*	4.0	2.0	1.5	0.6	0.3	5.0
20 < 50	7.0	3.5	2.5	1.0	0.5	8.0
50 < 100	10.0	4.5	4.0	1.5	0.7	12.0
100 < 1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

(Source: Anon., 2014)

*All power generation equipment's are limited to these values of current distortion, regardless of actual I_{SC}/I_L.

where, h = harmonic order

I_{SC} = maximum short circuit current at point-of-common-coupling

I_L = maximum demand load current (fundamental frequency) at point of common coupling

TDD = total demand distortion in % of maximum demand

APPENDIX B

C-SOURCE CODES FOR THE CONTROL SYSTEM

File: ControlSystem26R2.c

```
1  /*
2  * File: ControlSystem26R2.c
3  *
4  * Code generated for Simulink model 'ControlSystem26R2'.
5  *
6  * Model version : 1.3
7  * Simulink Coder version : 8.12 (R2017a) 16-Feb-2017
8  * C/C++ source code generated on : Wed Mar 06 12:40:40 2019
9  *
10 * Target selection: ert.tlc
11 * Embedded hardware selection: Intel->x86-64 (Windows64)
12 * Code generation objectives:
13 * 1. Execution efficiency
14 * 2. RAM efficiency
15 * Validation result: Not run
16 */
18 #include "ControlSystem26R2.h"
20 /* Private macros used by the generated code to access rt Model */
21 #ifndef rtmIsMajorTimeStep
22 # define rtmIsMajorTimeStep(rtm) (((rtm)->Timing.simTimeStep) ==
   MAJOR_TIME_STEP)
23 #endif
25 #ifndef rtmIsMinorTimeStep
26 # define rtmIsMinorTimeStep(rtm) (((rtm)->Timing.simTimeStep) ==
   MINOR_TIME_STEP)
27 #endif
29 #ifndef rtmGetTPtr
30 # define rtmGetTPtr(rtm) ((rtm)->Timing.t)
31 #endif
33 #ifndef rtmSetTPtr
34 # define rtmSetTPtr(rtm, val) ((rtm)->Timing.t = (val))
35 #endif
37 /* Continuous states */
38 X rtX;
40 /* Block signals and states (auto storage) */
41 DW rtDW;
```

```
43  /* Real-time model */
44  RT_MODEL rtM_;
45  RT_MODEL *const rtM = &rtM_;
47  /* private model entry point functions */
48  extern void ControlSystem26R2_derivatives(void);
50  /*
51  * This function updates continuous states using the ODE3 fixed-step
52  * solver algorithm
53  */
54  static void rt_ertODEUpdateContinuousStates (RTWSolverInfo *si)
55  {
56  /* Solver Matrices */
57  static const real_T rt_ODE3_A[3] = {
58  1.0/2.0, 3.0/4.0, 1.0
59  };
61  static const real_T rt_ODE3_B[3][3] = {
62  { 1.0/2.0, 0.0, 0.0 },
64  { 0.0, 3.0/4.0, 0.0 },
66  { 2.0/9.0, 1.0/3.0, 4.0/9.0 }
67  };
69  time_T t = rtsiGetT(si);
70  time_T tnew = rtsiGetSolverStopTime(si);
71  time_T h = rtsiGetStepSize(si);
72  real_T *x = rtsiGetContStates(si);
73  ODE3_IntgData *id = (ODE3_IntgData *) rtsiGetSolverData(si);
74  real_T *y = id->y;
75  real_T *f0 = id->f[0];
76  real_T *f1 = id->f[1];
77  real_T *f2 = id->f[2];
78  real_T hB[3];
79  int_T i;
80  int_T nXc = 8;
81  rtsiSetSimTimeStep(si, MINOR_TIME_STEP);
83  /* Save the state values at time t in y, we'll use x as ynew. */
84  (void) memcpy(y, x,
85  (uint_T)nXc*sizeof(real_T));
87  /* Assumes that rtsiSetT and Model Outputs are up-to-date */
88  /* f0 = f(t,y) */
89  rtsiSetdX(si, f0);
90  ControlSystem26R2_derivatives ();
92  /* f(:,2) = feval(odefile, t + hA(1), y + f*hB(:,1), args(:)(*)); */
```

```
93  hB[0] = h * rt_ODE3_B[0][0];
94  for (i = 0; i < nXc; i++) {
95  x[i] = y[i] + (f0[i]*hB[0]);
96  }
98  rtsiSetT(si, t + h*rt_ODE3_A[0]);
99  rtsiSetdX(si, f1);
100 ControlSystem26R2_step();
101 ControlSystem26R2_derivatives();
103 /* f(:,3) = feval(odefile, t + hA(2), y + f*hB(:,2), args(:)(*)); */
104 for (i = 0; i <= 1; i++) {
105 hB[i] = h * rt_ODE3_B[1][i];
106 }
108 for (i = 0; i < nXc; i++) {
109 x[i] = y[i] + (f0[i]*hB[0] + f1[i]*hB[1]);
110 }
112 rtsiSetT(si, t + h*rt_ODE3_A[1]);
113 rtsiSetdX(si, f2);
114 ControlSystem26R2_step();
115 ControlSystem26R2_derivatives();
117 /* tnew = t + hA(3);
118 ynew = y + f*hB(:,3); */
119 for (i = 0; i <= 2; i++) {
120 hB[i] = h * rt_ODE3_B[2][i];
121 }
123 for (i = 0; i < nXc; i++) {
124 x[i] = y[i] + (f0[i]*hB[0] + f1[i]*hB[1] + f2[i]*hB[2]);
125 }
127 rtsiSetT(si, tnew);
128 rtsiSetSimTimeStep(si,MAJOR_TIME_STEP);
129 }
131 /* Model step function */
132 void ControlSystem26R2_step(void)
133 {
134 real_T rtb_Integrator;
135 if (rtmIsMajorTimeStep(rtM)) {
136 /* set solver stop time */
137 rtsiSetSolverStopTime(&rtM->solverInfo,((rtM->Timing.clockTick0+1)*
138 rtM->Timing.stepSize0));
139 } /* end Major Time Step */
141 /* Update absolute time of base rate at minor time step */
142 if (rtmIsMinorTimeStep(rtM)) {
```

```
143  rtM->Timing.t[0] = rtsiGetT(&rtM->solverInfo);
144  }
146  /* Sum: '<Root>/Sum4' incorporates:
147  * Constant: '<Root>/Load Current '
148  * Constant: '<Root>/Source Current'
149  * TransferFcn: '<Root>/RL Filter Circuit'
150  */
151  rtDW.Sum4 = (10.526315789473685 * rtX.RLFilterCircuit_CSTATE + 1.0) - 1.0;
153  /* Sum: '<Root>/Sum' incorporates:
154  * Constant: '<Root>/Vdc-ref'
155  * TransferFcn: '<Root>/Nonlinear Load and Capacitor'
156  */
157  rtb_Integrator = 650.0 - (0.0 * rtX.NonlinearLoadandCapacitor_CSTAT[0] +
158  5.0E+7 * rtX.NonlinearLoadandCapacitor_CSTAT[1]);
160  /* Gain: '<S1>/Integral Gain' */
161  rtDW.IntegralGain = 1014.6 * rtb_Integrator;
163  /* Sum: '<Root>/Sum1' incorporates:
164  * Gain: '<Root>/Gain1'
165  * Gain: '<S1>/Proportional Gain'
166  * Integrator: '<S1>/Integrator'
167  * Sum: '<S1>/Sum'
168  */
169  rtb_Integrator = (181.14 * rtb_Integrator + rtX.Integrator_CSTATE) - 0.5 *
170  rtDW.Sum4;
172  /* Gain: '<S2>/Integral Gain' */
173  rtDW.IntegralGain_o = 0.321453135977634 * rtb_Integrator;
175  /* TransferFcn: '<Root>/PWM Inverter' */
176  rtDW.PWMInverter = 0.0;
177  rtDW.PWMInverter += 2702.7027027027029 * rtX.PWMInverter_CSTATE;
179  /* Sum: '<Root>/Sum3' incorporates:
180  * Gain: '<Root>/Gain2'
181  * Gain: '<S2>/Proportional Gain'
182  * Integrator: '<S2>/Integrator'
183  * Sum: '<S2>/Sum'
184  * TransferFcn: '<Root>/Nonlinear Load and Capacitor1'
185  */
186  rtDW.Sum3 = (0.175050208296888 * rtb_Integrator + rtX.Integrator_CSTATE_i) -
187  (0.0 * rtX.NonlinearLoadandCapacitor1_CSTA[0] + 5.0E+7 *
188  rtX.NonlinearLoadandCapacitor1_CSTA[1]) * 0.5;
189  if (rtmIsMajorTimeStep(rtM)) {
190  rt_ertODEUpdateContinuousStates(&rtM->solverInfo);
```

```
192  /* Update absolute time for base rate */
193  /* The "clockTick0" counts the number of times the code of this task has
194   * been executed. The absolute time is the multiplication of "clockTick0"
195   * and "Timing.stepSize0". Size of "clockTick0" ensures timer will not
196   * overflow during the application lifespan selected.
197   */
198  ++rtM->Timing.clockTick0;
199  rtM->Timing.t[0] = rtsiGetSolverStopTime(&rtM->solverInfo);
201  {
202  /* Update absolute timer for sample time: [0.008s, 0.0s] */
203  /* The "clockTick1" counts the number of times the code of this task has
204   * been executed. The resolution of this integer timer is 0.008, which is the step size
205   * of the task. Size of "clockTick1" ensures timer will not overflow during the
206   * application lifespan selected.
207   */
208  rtM->Timing.clockTick1++;
209  }
210  } /* end MajorTimeStep */
211  }
213  /* Derivatives for root system: '<Root>' */
214  void ControlSystem26R2_derivatives(void)
215  {
216  XDot *_rtXdot;
217  _rtXdot = ((XDot *) rtM->derivs);
219  /* Derivatives for TransferFcn: '<Root>/RL Filter Circuit' */
220  _rtXdot->RLFilterCircuit_CSTATE = 0.0;
221  _rtXdot->RLFilterCircuit_CSTATE += -84.21052631578948 *
222  rtX.RLFilterCircuit_CSTATE;
223  _rtXdot->RLFilterCircuit_CSTATE += rtDW.PWMInverter;
225  /* Derivatives for TransferFcn: '<Root>/Nonlinear Load and Capacitor1' */
226  _rtXdot->NonlinearLoadandCapacitor1_CSTA[0] = 0.0;
227  _rtXdot->NonlinearLoadandCapacitor1_CSTA[0] += -1.0E+7 *
228  rtX.NonlinearLoadandCapacitor1_CSTA[0];
229  _rtXdot->NonlinearLoadandCapacitor1_CSTA[1] = 0.0;
230  _rtXdot->NonlinearLoadandCapacitor1_CSTA[0] += -0.0 *
231  rtX.NonlinearLoadandCapacitor1_CSTA[1];
232  _rtXdot->NonlinearLoadandCapacitor1_CSTA[1] +=
233  rtX.NonlinearLoadandCapacitor1_CSTA[0];
234  _rtXdot->NonlinearLoadandCapacitor1_CSTA[0] += rtDW.Sum4;
236  /* Derivatives for TransferFcn: '<Root>/Nonlinear Load and Capacitor' */
237  _rtXdot->NonlinearLoadandCapacitor_CSTAT[0] = 0.0;
```

```
238  _rtXdot->NonlinearLoadandCapacitor_CSTAT[0] += -1.0E+7 *
239  rtX.NonlinearLoadandCapacitor_CSTAT[0];
240  _rtXdot->NonlinearLoadandCapacitor_CSTAT[1] = 0.0;
241  _rtXdot->NonlinearLoadandCapacitor_CSTAT[0] += -0.0 *
242  rtX.NonlinearLoadandCapacitor_CSTAT[1];
243  _rtXdot->NonlinearLoadandCapacitor_CSTAT[1] +=
244  rtX.NonlinearLoadandCapacitor_CSTAT[0];
245  _rtXdot->NonlinearLoadandCapacitor_CSTAT[0] += rtDW.Sum4;
247  /* Derivatives for Integrator: '<S1>/Integrator' */
248  _rtXdot->Integrator_CSTATE = rtDW.IntegralGain;
250  /* Derivatives for Integrator: '<S2>/Integrator' */
251  _rtXdot->Integrator_CSTATE_i = rtDW.IntegralGain_o;
253  /* Derivatives for TransferFcn: '<Root>/PWM Inverter' */
254  _rtXdot->PWMInverter_CSTATE = 0.0;
255  _rtXdot->PWMInverter_CSTATE += -2702.7027027027029 *
     rtX.PWMInverter_CSTATE;
256  _rtXdot->PWMInverter_CSTATE += rtDW.Sum3;
257  }
259  /* Model initialize function */
260  void ControlSystem26R2_initialize(void)
261  {
262  /* Registration code */
263  {
264  /* Setup solver object */
265  rtsiSetSimTimeStepPtr(&rtM->solverInfo, &rtM->Timing.simTimeStep);
266  rtsiSetTPtr(&rtM->solverInfo, &rtmGetTPtr(rtM));
267  rtsiSetStepSizePtr(&rtM->solverInfo, &rtM->Timing.stepSize0);
268  rtsiSetdXPtr(&rtM->solverInfo, &rtM->derivs);
269  rtsiSetContStatesPtr(&rtM->solverInfo, (real_T **) &rtM->contStates);
270  rtsiSetNumContStatesPtr(&rtM->solverInfo, &rtM->Sizes.numContStates);
271  rtsiSetNumPeriodicContStatesPtr(&rtM->solverInfo,
272  &rtM->Sizes.numPeriodicContStates);
273  rtsiSetPeriodicContStateIndicesPtr(&rtM->solverInfo,
274  &rtM->periodicContStateIndices);
275  rtsiSetPeriodicContStateRangesPtr(&rtM->solverInfo,
276  &rtM->periodicContStateRanges);
277  rtsiSetErrorStatusPtr(&rtM->solverInfo, (&rtmGetErrorStatus(rtM)));
278  rtsiSetRTModelPtr(&rtM->solverInfo, rtM);
279  }
281  rtsiSetSimTimeStep(&rtM->solverInfo, MAJOR_TIME_STEP);
282  rtM->intgData.y = rtM->odeY;
```

```
283  rtM->intgData.f[0] = rtM->odeF[0];
284  rtM->intgData.f[1] = rtM->odeF[1];
285  rtM->intgData.f[2] = rtM->odeF[2];
286  rtM->contStates = ((X *) &rtX);
287  rtsiSetSolverData(&rtM->solverInfo, (void *)&rtM->intgData);
288  rtsiSetSolverName(&rtM->solverInfo,"ode3");
289  rtmSetTPtr(rtM, &rtM->Timing.tArray[0]);
290  rtM->Timing.stepSize0 = 0.008;
292  /* InitializeConditions for TransferFcn: '<Root>/RL Filter Circuit' */
293  rtX.RLFilterCircuit_CSTATE = 0.0;
295  /* InitializeConditions for TransferFcn: '<Root>/Nonlinear Load and Capacitor1'
     */
296  rtX.NonlinearLoadandCapacitor1_CSTA[0] = 0.0;
298  /* InitializeConditions for TransferFcn: '<Root>/Nonlinear Load and Capacitor' */
299  rtX.NonlinearLoadandCapacitor_CSTAT[0] = 0.0;
301  /* InitializeConditions for TransferFcn: '<Root>/Nonlinear Load and Capacitor1'
     */
302  rtX.NonlinearLoadandCapacitor1_CSTA[1] = 0.0;
304  /* InitializeConditions for TransferFcn: '<Root>/Nonlinear Load and Capacitor' */
305  rtX.NonlinearLoadandCapacitor_CSTAT[1] = 0.0;
307  /* InitializeConditions for Integrator: '<S1>/Integrator' */
308  rtX.Integrator_CSTATE = 0.0;
310  /* InitializeConditions for Integrator: '<S2>/Integrator' */
311  rtX.Integrator_CSTATE_i = 0.0;
313  /* InitializeConditions for TransferFcn: '<Root>/PWM Inverter' */
314  rtX.PWMInverter_CSTATE = 0.0;
315  }
317  /*
318  * File trailer for generated code.
319  *
320  * [EOF]
321  */
```

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W